Report 11421 9 March 1999

GENCORP AEROJET

Integrated Advanced Microwave Sounding Unit-A (AMSU-A)

Performance Verification Report AMSU-A1 Antenna Drive Subsystem P/N 1331720-2, S/N 107

Contract No. NAS 5-32314 CDRL 208

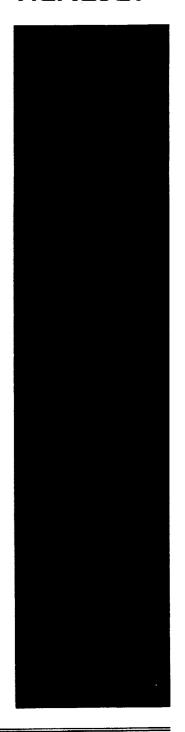
Submitted to:

National Aeronautics and Space Administration Goddard Space Flight Center Greenbelt, Maryland 20771

Submitted by:

Aerojet 1100 West Hollyvale Street Azusa, California 91702





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Integrated Advanced Microwave Sounding Unit-A (AMSU-A)

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AMSU-A VERIFICATION TEST REPORT

TEST ITEM:

AMSU- A1 ANTENNA DRIVE SUBSYSTEM

PART OF P/N: 1331720-2 SERIAL NUMBER: 107

LEVEL OF ASSEMBLY:

SUBASSEMBLY AND COMPLETE INSTRUMENT

ASSEMBLY

TYPE HARDWARE:

FLIGHT

VERIFICATION:

AE-26002/1E

PROCEDURE NO.

TEST DATE:

SUBSYSTEM:

START DATE: 27 Jan 1999

FINISH DATE:

17 Feb 1999

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1.0 INTRODUCTION

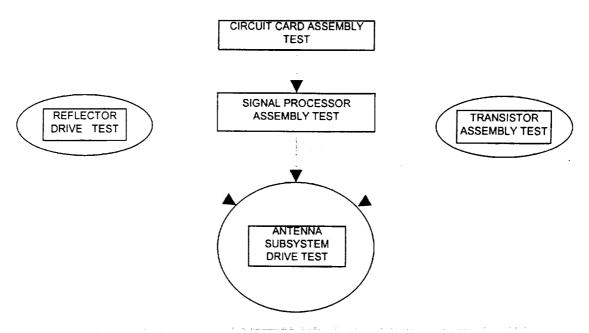
An antenna drive subsystem test was performed on the METSAT AMSU-A1, S/N 107 instrument. The objective of the test was to demonstrate compliance with applicable paragraphs of AMSU-A specifications S-480-80. Tests were conducted at both the subassembly and instrument level.

2.0 SUMMARY

The antenna drive subsystem of the METSAT AMSU-A1, S/N 107, P/N 1331720-2, completed acceptance testing per AES Test Procedure AE-26002/1E. The test included: Scan Motion and Jitter, Pulse Load Bus Peak Current and Rise Time, Resolver Reading and Position Error, Gain/Phase Margin, and Operational Gain Margin.

The drive motors and electronic circuitr

y were also tested at the component level. The drive motor test includes: Starting Torque Test, Motor Commutation Test, Resolver Operation/ No-Load Speed Test, and Random Vibration. The electronic circuitry was tested at the Circuit Card Assembly (CCA) level of production; each test exercised all circuit functions. The transistor assembly was tested during the W3 cable assembly (1356941-1) test. Refer to Figure 1 for test flow.



Antenna Subsystem and Subsystem Component Test Flow Figure 1.

The antenna drive subsystem satisfactorily passed all of the performance requirements. There were no failures in any of the antenna drive components during subsystem testing.

The results of the subsystem and component level testing are discussed in more detail in the following sections:

Reflector Drive Assembly	5.1
Circuit Card Assemblies	5.2
Signal Processor	5.3
Transistor Assembly	5.4
Antenna Drive Subsystem	5.5

3.0 TEST CONFIGURATION

The *Reflector Drive Assembly Tests* confirm the operability of the motor under test. The test configuration includes the motor, motor shaft, bearings, and a supporting housing.

The Circuit Card Assembly (CCA) Tests confirm the operability of each CCA. Each test includes the CCA under test, electronic test fixtures, and the necessary loads.

A segment of the *Signal Processor Tests* ensures the scan drive electronics are functioning properly prior to its assembly into the instrument. The test configuration includes:

- Timing and Control CCA
- Scan Control Interface CCA
- Relay Driver and Current Monitor CCA
- Interface Converter CCA
- Resolver Data Isolator CCA
- R/D Converter CCA
- Motor Driver CCA
- Test fixture and cabling to simulate the spacecraft bus interface
- Test fixture and cabling to interrogate and analyze positional data
- Test motor and inertia wheel

The *Transistor Assembly Test* verifies the correct wiring of the transistor assembly and associated cabling. Test configuration includes the CKT 1000 (continuity and Hi-Pot tester), and test fixtures.

The Antenna Drive Subsystem Tests:

- Are configured with the same motor control CCA's used in the signal processor test, interconnecting wiring, the power transistor assembly, and the drive assembly with reflector.
- The antenna drive subsystem components were all installed in the instrument when the subsystem test was performed.

• DC power for the motor control circuit cards was provided by a DC/DC converter simulator P/N: 1359322-1. The simulator operates on 120VAC facility supplied power. The power for the reflector motor drive circuits however was provided directly by the STE 28V Bus power supply.

4.0 TEST SETUP

The antenna drive subsystem tests are performed during system integration. During system integration testing, the instrument is proven electrically safe via ground isolation, and power distribution checks. Next, the communication link is exercised to ensure commands are received and interpreted correctly. The Antenna Drive Subsystem Test is then performed.

5.0 TEST RESULTS

The Antenna Drive Subsystem components designated for use in the METSAT AMSU-A1 instrument are shown in Table 1.

CCA (A1-1)	S/N
Resolver Data Isolator Assembly (A1-1)	F21
Interface Converter Assembly (A1-1)	F27
Motor Driver Assembly (A1-1)	F04
R/D Converter/ Oscillator Assembly (A1-1)	F22

CCA (A1-2)	S/N
Resolver Data Isolator Assembly (A1-2)	F31
Interface Converter Assembly (A1-2)	F34
Motor Driver Assembly (A1-2)	F11
R/D Converter/ Oscillator Assembly (A1-2)	F25

OTHER	S/N
Reflector Drive Motor (A1-1)	F11
Reflector Drive Motor (A1-2)	F10
Signal Processor	F03

Table 1.

METSAT AMSU-A1 S/N: 107 Antenna
Subsystem Component S/N Designations

All components designated for use in the METSAT AMSU-A1 instrument (pertaining to the scan drive circuitry) passed on the first time through component testing.

5.1 REFLECTOR DRIVE ASSEMBLIES

The tests performed on this unit are: Starting Torque Test, Motor Commutation Test, Resolver Operation/ No-Load Speed Test, and Random Vibration. The Motor Commutation and Resolver Operation tests are performed both pre and post-vibration.

Starting Torque

Both reflector drive assemblies (F10 and F11) passed the starting torque test at ambient temperature as well as at the colder plateaus first time through testing.

Motor Commutation Test

This test is performed to determine the commutation characteristics of the motor under test. Both reflector drive assemblies (F10 and F11) passed the motor commutation test both pre- and post-vibration tests without incident.

Resolver Operation/ No-Load Speed Test

This test is performed to verify resolver operation as well as speed characteristics and back electromotive force of the motor. Both reflector drive assemblies (F10 and F11) passed the resolver operation/ no-load speed test both pre- and post-vibration tests without incident.

Random Vibration

Reflector drive assemblies (F10 and F11) passed vibration testing first time through. The motor assembly also passed the pre- and post-vibration electronic tests as well as the post-vibration visual inspection without incident.

5.2 CIRCUIT CARD ASSEMBLIES

Test procedures were prepared for each motor control circuit card; document revision status is controlled by reference in the shop order. The cards were individually tested to the procedures and results were recorded on data sheets found in Appendix A. The following list indexes the CCA Test Data Sheets:

- Appendix A1 Resolver Data Isolator Assembly (A1-1)
- Appendix A2..... Resolver Data Isolator Assembly (A1-2)
- Appendix A3..... Interface Converter Assembly (A1-1)
- Appendix A4..... Interface Converter Assembly (A1-2)

- Appendix A5..... Motor Driver Assembly (A1-1)
- Appendix A6...... Motor Driver Assembly (A1-2)
- Appendix A8......R/D Converter/ Oscillator Assembly (A1-2)

All circuit card assemblies passed testing the first time through. The assembly build shop orders contain the part number and accept tag record the of test and select resistors.

5.3 SIGNAL PROCESSOR

For the first time, the entire antenna drive motor electronics is mated together. The test instrumentation commands and interrogates the electronics during this segment of testing. The instrumentation sends position commands to the Interface Converter CCA. The Interface Converter D/A's the command and provides inputs to the Motor Driver CCA. The test motor (instrumentation) responds to the drive signal and feeds back positional data via resolver outputs. The instrumentation then interrogates the Resolver Data Isolator CCA for position data. A comparison is made in the instrumentation between the position command sent and the actual position received. The pass/ fail indication is presented to the operator for test data sheet recording.

The signal processor assembly (F03) passed all scan drive tests.

5.4 TRANSISTOR ASSEMBLY

All transistor assemblies are tested along with their respective W3 cable. The cable is continuity, then hi-pot tested prior to attaching the transistor circuitry. Each transistor pair is exercised validating the turn on voltage, current drawn, and cable wiring as well.

The W3 cable and transistor assembly underwent component testing and passed without incident.

5.5 ANTENNA SUBSYSTEM DRIVE TESTS

The antenna drive motor electronics mates with the instrument microprocessor for the first time during this segment of testing. The microprocessor sends position commands from the memory CCA to the Interface Converter CCA. The Interface Converter D/A's the command and provides inputs to the Motor Driver CCA. The Reflector Drive Motor responds to the drive signals and feeds back positional data via the resolver outputs. The microprocessor then interrogates the Resolver Data Isolator CCA for position data. The microprocessor in turn communicates with the spacecraft interface.

During other segments of the test, positional data is monitored via a potentiometer attached to the shaft of each reflector drive assembly. This provides scan characteristic information in regard to overshoot, jitter, and beam position transition timing for each motor assembly.

The remaining paragraphs in this section discuss tests that ensures the instrument complies with specific operating parameters. Prior to conducting these tests there is a series of preliminary checks that are run to select component values that customize the operating parameters of each motor. These checks perform the following functions:

- Program "on board" memory with Beam Position Pointing Angles for each reflector drive assembly
- Adjust for peak Motor Current Limits on both A1-1 and A1-2 motor drive circuits
- Observe Preliminary Scan Dynamics on both A1-1 and A1-2 motor drive circuits
- Identify Mechanical Resonant Frequencies of each reflector drive assembly

Beam Position Pointing Angles are calculated from Nadir pointing direction which is determined on the antenna range. The instrument's EPROMs (EPROMs for testing; PROMs for final configuration) are programmed to reflect the position commands. The initial programming may require fine tuning; fine tuning is determined during the remaining segments of the test procedure.

Motor Current Limits were adjusted, via selecting "test and select" resistors, to comply with the specification requirement; less than 1.1 amp peak current.

Preliminary Scan Dynamics looked good; transition times, overshoot and jitter were all acceptable at the sampled pointing directions (5).

The *Mechanical Resonant Frequencies* were identified; notch filters were calculated and installed to compensate for these resonant frequencies.

5.5.1 SCAN MOTION AND JITTER

In this test, the antenna position was measured in a series of five 8-sec full scans. The measurement was made with a 1-turn test potentiometer temporarily affixed to the rear end of the motor shaft. A Dynamic Signal Analyzer (DSA) was connected to the pot wiper to record the antenna position data. Five scans of each A1-1 and A1-2 were captured and stored on the AMSU-A1 Test Data File disc. One representative waveform from each subassembly is presented in Appendix B1 (A1-1) and Appendix B34 (A1-2).

Each 3.33 degrees scene step was expanded and checked for both a 35 msec max step time, and a 165 msec integration period. Expanded waveforms were plotted and are presented in Appendix B2 thru B31 for the A1-1 subassembly and Appendix B35 thru

B64 for the A1-2 subassembly. All of the scene steps meet the step response requirement for transition time, overshoot, and jitter.

Slew periods to the cold and warm calibration stations were measured and met requirements. A time of 0.21 sec is allocated for the 35.0 degree slew to cold cal, and 0.40 sec for the 96.67 degree slew to warm cal. Calibration station jitter was less than the \pm 5 % maximum permitted. Expanded waveforms for each subassembly were plotted and are presented in Appendix B32 and B33 (A1-1) and Appendix B65 and B66 (A1-2). The waveforms are also stored on the AMSU-A1 Test Data File disc. The test data sheets are presented in Appendix B67 (A1-1) and B68 (A1-2).

5.5.2 PULSE LOAD BUS PEAK CURRENT AND RISE TIME

The Pulse Load pulse load bus peak current and the rate of change of current were measured. The peak current must be less than 1A at any beam position along the scan. Peak current along the scan is .9368A. The current rate of change while transitioning from one beam position to the next (including the transition to the cold calibration and warm calibration targets) should be greater than 35 microseconds. A random 3.33° step was selected; the transition to the next step was 2.344 ms. The transition to the warm cal position start and stop was significantly longer than the required 35 ms; 1.953 and 2.344 ms, respectively.

The peak bus current was measured across the entire scan and met the requirement. The full scan waveform was plotted and is presented in Appendix C1. The waveform is also stored on the AMSU-A1 Test Data File disc. The test data sheet is presented in Appendix C2.

5.5.3 RESOLVER READING AND POSITION ERROR

The 14-bit command position word is stored in the "on-board" memory and is read to the motor drive circuitry under microprocessor program control. The microprocessor also reads the resolver output at each of the thirty scene stations, and at the cold and warm calibration positions. The readings are made at the start of integration (LOOK 1), and halfway into the integration period (LOOK 2). The resolver data is sent to the spacecraft interface for subsequent transmission to the STE.

The purpose of this portion of the test is to demonstrate that the antenna is meeting beam pointing requirements.

If the antenna is out of the pointing tolerance of $> \pm 5$ counts at LOOK 2, the EPROM is reprogrammed to bring the pointing direction to within the prescribed tolerances. A copy of the STE computer print out showing the pointing direction is shown in Figure 2 for the A1-1 subassembly and Figure 3 for the A1-2 subassembly.

Difference*

Look2

ī

-2

-1

Look I

-1

-1

Look2

		Ac	tual	Diffe	ence*			1
BP	Command	Look i	Look2	Look 1	Look2	BP	Command	Look 1
1	16251	16253	16253	2	2	17	2294	2298
2	19	17	19	-2	0	18	2446	2448
3	171	168	171	-3	0	19	2597	2598
4	322	323	323	1	1	20	2749	2750
5	474	473	473	-1	-1	21	2901	2901
6	626	623	625	-3	-1	22	3052	3051
7	777	779	778	2	1	23	3204	3205
8	929	931	930	2	l	24	3356	3355
9	1081	1081	1080	0	-1	25	3507	3511
10	1232	1234	1234	2	2	26	3659	3662
11	1384	1384	1384	0	0	27	3811	3811
12	1536	1538	1537	2	1	28	3962	3965
13	1687	1688	1688	1	1	29	4114	4115
14	1839	1840	1840	1	I	30	4266	426 7
15	1991	1991	1992	0	1	Œ1	5860	586 0
16	2142	2145	2144	3	2	WC	10259	10258

Figure 2. Beam Position Pointing Directions and Error Calculation for A1-1

		Actual		Difference*			1 1	Actual		Difference*	
ВP	Command	Look 1	Look2	Look!	Look2	B₽	Command	Look 1	Look2	Look 1	Look2
ì	403	401	401	-2	-2	17	2830	2829	2828	-1	-2
2	555	553	554	-2	-l	18	2982	2987	2984	5	2
3	707	711	709	4	2	19	3133	3130	3133	-3	0
4	858	856	858	-2	0	20	3285	3287	3287	2	2
5	1010	1011	1012	1	2	21	3437	3441	3439	4	2
6	1162	1161	1161	-1	-]	22	3588	3588	3590	0	2
7	1313	1314	1315]	2	23	3740	3737	3738	-3	-2
8	1465	1467	1466	2	1	24	3892	3894	3894	2	2
9	1617	1619	1618	2	1	25	4043	4044	4045	1	2
10	1768	1765	1766	-3	-2	2 6	4195	4195	4197	0	2
11	1920	1923	1921	3	l	27	4347	4344	4346	-3	-1
12	2072	2071	2070	-1	-2	28	4498	4497	4500	-1	2
13	2223	2221	2225	-2	2	29	4650	4651	4652	1	2
14	2375	2373	2375	-2	0	30	4802	4806	4804	4	2
15	2527	2528	2529	1	2	Œ1	6396	6399	6399	3	3
16	2678	2680	2680	2	2	WC	10795	10794	10794	-1	-]
				Difference b	oetween Comm	and and Actu	al				

Figure 3. Beam Position Pointing Directions and Error Calculation for A1-2

5.5.4 GAIN/PHASE MARGIN

A gain/phase margin test was performed on the antenna drive subsystem. The test was performed by obtaining a Bode plot of the control loop and measuring the gain at 180° phase differential and the phase margin at the 0db crossover point.

The Dynamic Signal Analyzer (DSA) was used to make the measurement operating in the swept sine mode. Three separate Bode plots were made on the antenna and the gain and phase margins were determined from each plot. The gain margin measured was 14.505 db (average of three) for the A1-1 subsystem and 14.226 db (average of three) for the A1-2 subsystem. The phase margin measured was 67.623° (average of three) for the A1-1 subsystem and 70.063° (average of three) for the A1-2 subsystem. These margins exceed the specification requirements of 9.2 db and 25 degrees and therefore are acceptable. The three Bode waveforms were plotted and are presented in Appendix D1 thru D3 for the A1-1 subsystem and Appendix D4 thru D6 for the A1-2 subsystem. The waveforms are also stored on the AMSU-A1 Test Data File disc. The test data sheets are presented in Appendix D7 and D8 for A1-1 and A1-2, respectively.

5.5.5 OPERATIONAL GAIN MARGIN

An operational gain margin test was performed on the instrument three times. This test consists of increasing the gain of the control loop until oscillation occurs. The gain increase and frequency of oscillation are measured. An increase in gain greater than 8 db is required; the frequency of oscillation is an observation.

A 50K pot was connected in series with the R58 feedback resistor on amplifier AR8. The resistance of the test pot was slowly added to the feedback resistor while observing the reflector for oscillations.

The reflector begins to produce an audible sound as gain is increased. The following added resistance values are calculated to have the following gain margins for the A1-1 and A1-2 subsystems:

Resistance	Gain		
(ohms)			
35.93 K	9.0 db		
37.34 K	9.2 db		
37.39 K	9.2 db		

A1-1

Resistance	Gain
(ohms)	
38.90 K	9.4 db
37.56 K	9.2 db
37.61 K	9.2 db
A	1-2

The first mode mechanical resonance of the shaft and reflector is about 95 Hz for the A1-1 subsystem. The power spectrum waveform was plotted and is presented in Appendix E1. The first mode mechanical resonance of the shaft and reflector is about 94 Hz for the A1-2 subsystem. The power spectrum waveform was plotted and is presented in Appendix E2. These waveforms are also stored on the AMSU-A1 Test Data File disc. The test data sheets are presented in Appendix E3 and E4 for the A1-1 and A1-2 subsystems respectively.

6.0 CONCLUSION

Based on the test results, it can be concluded that the METSAT AMSU-A1 S/N 107 antenna drive subsystem meets the AMSU-A specification requirements.

7.0 TEST DATA

Test data for the METSAT AMSU-A1 S/N 107 obtained in the antenna drive subsystem test is attached. Data sheet number and type of test is shown in the following Appendix Index.

APPENDIX INDEX

Appendix A1 Resolver Data Isolator CCA TDS (A1-1)
Appendix A2 Resolver Data Isolator CCA TDS (A1-2)
Appendix A3 Interface Converter CCA TDS (A1-1)
Appendix A4 Interface Converter CCA TDS (A1-2)
Appendix A5 Motor Driver CCA TDS (A1-1)
Appendix A6 Motor Driver CCA TDS (A1-2)
Appendix A7R/D Converter/ Oscillator CCA TDS (A1-1)
Appendix A8
Appendix B1Full Scan Step Response (A1-1)
Appendix B1Full Scan Step Response (A1-1) Appendix B2 thru B31Single Step Responses (A1-1)
Appendix B2 thru B31 Single Step Responses (A1-1)
Appendix B2 thru B31 Single Step Responses (A1-1) Appendix B32 Cold Calibration Step Response (A1-1)
Appendix B2 thru B31 Single Step Responses (A1-1) Appendix B32 Cold Calibration Step Response (A1-1) Appendix B33 Warm Calibration Step Response (A1-1)
Appendix B2 thru B31 Single Step Responses (A1-1) Appendix B32 Cold Calibration Step Response (A1-1) Appendix B33 Warm Calibration Step Response (A1-1) Appendix B34 Full Scan Step Response (A1-2)
Appendix B2 thru B31 Single Step Responses (A1-1) Appendix B32 Cold Calibration Step Response (A1-1) Appendix B33 Warm Calibration Step Response (A1-1) Appendix B34 Full Scan Step Response (A1-2) Appendix B35 thru B64 Single Step Responses (A1-2)
Appendix B2 thru B31 Single Step Responses (A1-1) Appendix B32 Cold Calibration Step Response (A1-1) Appendix B33 Warm Calibration Step Response (A1-1) Appendix B34 Full Scan Step Response (A1-2) Appendix B35 thru B64 Single Step Responses (A1-2) Appendix B65 Cold Calibration Step Response (A1-2)

Appendix C1Peak Pulse Load Bus Current Waveform
Appendix C2Pulse Load Bus Current TDS
Appendix D1 thru D3Gain/Phase Margin Bode Plots (A1-1)
Appendix D4 thru D6Gain/Phase Margin Bode Plots (A1-2)
Appendix D7Gain/ Phase Margin TDS (A1-1)
Appendix D8Gain/ Phase Margin TDS (A1-2)
Appendix E1Operational Gain Margin Power Spectrum (A1-1)
Appendix E2Operational Gain Margin Power Spectrum (A1-2)
Appendix E3Operational Gain Margin TDS (A1-1)
Appendix E4Operational Gain Margin TDS (A1-2)

APPENDIX A

TEST DATA SHEETS FOR SCAN DRIVE CIRCUIT CARD ASSEMBLIES

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				-
		•		
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TEST DATA SHEET B-6 (Sheet 1 of 2)

RESOLVER DATA ISOLATOR CCA (P/N 1334972) (Paragraph 6.6.7)

Date:

7/28/97

S/N:

F21 1334972-1

6.6.7.1 Supply Voltages

Supply*	Measured Value (V)	Limits (Vdc)	Pass/Fail
+5 V (I)	75.06V	± 0.25	$\frac{1}{2}$
+5 V (U)	75.00 V	± 0.25	<u> </u>

6.6.7.2 Supply Currents

Steps 1 and 2:

Supply*	Measured Value (mA)	Limits (mA)	Pass/Fail
+5 V (I)	53.49	100 max	<u> </u>
+5 V (U)	3 2 3 . 70	400 max	<u> </u>

Steps 3 and 4:

-	Supply*	Measured Value (mA)	Limits (mA)	Pass/Fail
	+5 V (I)	83.05	150 max	1 1
	+5 V (U)	12.11	30 max	<u> </u>

^{*} I = Isolated, U = Unisolated

6.6.7.3 Resolver Data

Bit No.	Pass/Fail
API 0 - AP Bit 0	P
API 1 - AP Bit 1	P
API 2 - AP Bit 2	f
API 3 - AP Bit 3	ę
API 4 - AP Bit 4	P
API 5 - AP Bit 5	f
API 6 - AP Bit 6	P
API 7 - AP Bit 7	P P
API 8 - AP Bit 8	<u> </u>
API 9 - AP Bit 9	f
API 10 - AP Bit 10	_
API 11 - AP Bit 11	F
API 12 - AP Bit 12	
API 13 - AP Bit 13	P

6.6.7.4 Converter Busy Pulse

Converter Busy Pulse	Measured Value (usec)	Limits (µsec)	Pass/Fail
15.0	14.6	± 3.0	<u> </u>

TEST DATA SHEET B-6 (Sheet 2 of 2)

RESOLVER DATA ISOLATOR CCA (P/N 1334972) (Paragraph 6.6.7)

		- 1
Comments: NON	6	
	.*	
Conducted by:	Test Engineer Date 7/23/17	
Verified by:	Quality Coapol Inspector Date	
Approved by:	DCMC Date	

TEST DATA SHEET B-6 (Sheet 1 of 2)

RESOLVER DATA ISOLATOR CCA (P/N 1334972) (Paragraph 6.6.7)

Date: 7/2497 S/N: F31 \334912-1

6.6.7.1 Supply Voltages

Supply*	Measured Value (V)	Limits (Vdc)	Pass/Fail
+5 V (I)	+5.00	± 0.25	<u> </u>
+5 V (U)	+5.06	± 0.25	ΙΡ

6.6.7.2 Supply Currents

Steps 1 and 2:

Supply*	Measured Value (mA)	Limits (mA)	Pass/Fail
+5 V (I)	53.44	100 max	P
+5 V (U)	316.59	400 max	

Steps 3 and 4:

<u></u>	Supply*	Measured Value (mA)	Limits (mA)	Pass/Fail
+5 V	<u> </u>	83. 07	150 max	1 0
+5 V	(-) (U)	12.00	30 max	

^{*} I = Isolated, U = Unisolated

6.6.7.3 Resolver Data

Bit No.	Pass/Fail
API 0 - AP Bit 0	P P
API 1 - AP Bit 1	P
API 2 - AP Bit 2	P
API 3 - AP Bit 3	P P
API 4 - AP Bit 4	P
API 5 - AP Bit 5	
API 6 - AP Bit 6	<u>l</u>
API 7 - AP Bit 7	<u> </u>
API 8 - AP Bit 8	P
API 9 - AP Bit 9	<u> </u>
API 10 - AP Bit 10	<u> </u>
API 11 - AP Bit 11	- β
API 12 - AP Bit 12	<u>f</u>
API 13 - AP Bit 13	ρ

6.6.7.4 Converter Busy Pulse

The state of the s

Converter Busy Pulse	Measured Value (usec)	Limits (µsec)	Pass/Fail	
15.0	14.6	± 3.0	<u></u>	,

TEST DATA SHEET B-6 (Sheet 2 of 2)

RESOLVER DATA ISOLATOR CCA (P/N 1334972) (Paragraph 6.6.7)

Comments:			
			·
a 1	Denie Len	1/28/97	
Conducted by: Verified by:	Test Engineer	Date 07/29/97	
Approved by:	Quality Control Inspector	Date Date	

TEST DATA SHEET B-13 (Sheet 1 of 3)

INTERFACE/CONVERTER CCA (P/N 1331697) (Paragraph 6.13.7)

6.13.7.1 Supply Voltages

Supply	Measured Value (Vdc)	Limits (Vdc)	Pass/Fail
+5V (U)	5.01	+5V± 0.05	1
+15V (I)	15.01	+15V± 0.15	P
-15V (I)	-14.97	-15V± 0.15	P
+5V (I)	5.02	+5V± 0.05	P

6.13.7.2 Supply Currents

Step 1 (CP and API Low):

Supply	Measured Value (mA)	Limits (mA)	Pass/Fail
+5V (U)	86.62	70 - 110	1 9
+5V (I)	3.40	1.5 - 5.5	P
+15V (I)	18.50	15 - 23	P
-15V (I)	21.16	18 - 26	<u> </u>

Step 2 (CP and API High):

Supply	Measured Value (mA)	Limits (mA)	Pass/Fail
+5V (U)	56.52	40 - 70	P
+5V (I)	23.97	18 - 30	1 8
+15V (I)	18.50	15 - 23	P
-15V (I)	21.16	18 - 26	Р

6.13.7.3 Amplifier Offsets

Amplifier	Measured Value (mV)	Limits (mV)	Pass/Fail
AR1	-0.02	0.0 ±0.15	P
AR2	-0.45	0.0 ±2.0	P

TEST DATA SHEET B-13 (Sheet 2 of 3)

INTERFACE/CONVERTER CCA (P/N 1331697) (Paragraph 6.13.7)

13.1.4 Subuaction and 2 1.	Conversion	2-10-97	± 0.0001 ± 0.000	60
		7-10-9-1	10.000 1 ± 0.000	30
ep 1:		· /.	//	
Actual Position (API)	Command Position (CP)	AR1 Output	Test Result	
MSB LSB	MSB LSB	Voltage Required (Vdc)	' (Vdc)	Pass/Fai
00000000000000	00000000000000	0.00000	-0.000020	
00000000000001	00000000000000	-0.00061	-0.000492	
0000000000010	00000000000000	-0.00122	-0.001124	· [
0000000000011	00000000000000	-0.00184	-0.001749	
0000000000100	00000000000000	-0.00245	-0.002378	- 1
0000000001000	00000000000000	-0.00490 ★	-0.004871	<u>_</u>
0000000010000	00000000000000	-0.00979 ★	-0.009913	
0000000100000	00000000000000	-0.01958 *	-0.019968	<u>_</u>
00000001000000	00000000000000	-0.03917 ★	_0.040c72	<u>;r</u>
00000010000000	. 000000000000000	-0.07834 ≯	-0.680279	—- <u>ř</u> –
00000100000000	00000000000000	-0.15667 ≯	-0.16065	<u> </u>
00001000000000	00000000000000	-0.31334 ★	-0.32147	<u></u>
0001000000000	00000000000000	-0.62669 ★	-0.64314	<u> </u>
0010000000000	00000000000000	-1.25338 *	-1.2365	<u>_</u>
0100000000000	00000000000000	-2. 5 0675 ★	-2.5732	<u></u>
100000000000000000* Tolerance on output vo	00000000000000	-5.01350 * umfumme 9-10-97	10.000 ± 0.000 ± 0.000	60
10000000000000000000000000000000000000	00000000000000000000000000000000000000	umfummed 9-10-97	± 0.000 ± 0.000	60
* Tolerance on output volep 2: Actual Position (API)	00000000000000000000000000000000000000	4mfummed 9-10-97 ARI Output	1 0.000 1 0.000 1 0.000 Test Result	30
# Tolerance on output volume 2: Actual Position (API) MSB LSB	00000000000000000000000000000000000000	ARI Output Voltage Required (Vgc)	10.000 1 0.000 1 0.000 Test Result (Vdc)	60
10000000000000000000000000000000000000	00000000000000000000000000000000000000	ARI Output Voltage Required (Vgc)/ 0.00000	1 0.000 ± 0.000 ± 0.000 / Test Result (Vdc) -0.00034	30
10000000000000000000000000000000000000	00000000000000000000000000000000000000	9-10-97 ARI Output Voltage Required (Vgc)/ 0.00000 0.00061	10.000 10.000 10.000 Test Result (Vdc) -0.00034 +0.00030	30
10000000000000000000000000000000000000	00000000000000000000000000000000000000	AR1 Output Voltage Required (Vdc)/ 0.00000 0.00061 0.00122	10.000 10.000 10.000 Test Result (Vdc) -0.00034 +0.00530 +0.001208	Pass/Fail
10000000000000000000000000000000000000	00000000000000000000000000000000000000	ARI Output Voltage Required (Vac)/ 0.00000 0.00061 0.00122 0.00184	10.000 10.000 10.000 Test Result (Vdc) -0.00034 +0.001208 +0.001208 +0.001208	Pass/Fail
10000000000000000000000000000000000000	00000000000000000000000000000000000000	ARI Output Voltage Required (Vgc)/ 0.00000 0.00061 0.00122 0.00184 0.00245	10.000 10.000 10.000 Test Result (Vdc) -0.00034 +0.001208 +0.001208 +0.001208 +0.001461	Pass/Fail
10000000000000000000000000000000000000	00000000000000000000000000000000000000	ARI Output Voltage Required (Vgc)/ 0.00000 0.00061 0.00122 0.00184 0.00245 0.00490 *	10.000 10.000 10.000 10.000 Test Result (Vdc) -0.00034 +0.001208 +0.001208 +0.002461 10.004471	Pass/Fail
10000000000000000000000000000000000000	00000000000000000000000000000000000000	AR1 Output Voltage Required (Vac) 0.00000 0.00061 0.00122 0.00184 0.00245 0.00490 * 0.00979 *	10.000 10.000 10.000 10.000 Test Result (Vdc) -0.00034 +0.001208 +0.001208 +0.001208 +0.001461 10.004411 +0.0034	Pass/Fail
10000000000000000000000000000000000000	00000000000000000000000000000000000000	ARI Output Voltage Required (Vac)/ 0.00000 0.00061 0.00122 0.00184 0.00245 0.00490 * 0.00979 * 0.01958 *	10.000 10.000 10.000 10.000 10.00034 10.001208 10.001208 10.001208 10.001208 10.001208 10.001208 10.001208 10.001208 10.001208 10.001208	Pass/Fail
10000000000000000000000000000000000000	00000000000000000000000000000000000000	ARI Output Voltage Required (Vgc)/ 0.00000 0.00061 0.00122 0.00184 0.00245 0.00490 * 0.00979 * 0.01958 * 0.03917 *	10.000 10.000 10.000 10.000 10.000 10.00034 10.001208 10.001208 10.001208 10.001208 10.001208 10.001208 10.001208 10.001208 10.001208 10.001208 10.001208	Pass/Fail
10000000000000000000000000000000000000	00000000000000000000000000000000000000	ARI Output Voltage Required (Vgc)/ 0.00000 0.00061 0.00122 0.00184 0.00245 0.00490 * 0.00979 * 0.01958 * 0.03917 * 0.07834 *	10.000 10.000 10.000 10.000 10.00034 10.0032 10.0034 10.0034 10.0034 10.04032 10.080367	Pass/Fail
10000000000000000000000000000000000000	00000000000000000000000000000000000000	AR1 Output Voltage Required (Vdc) 0.00000 0.00061 0.00122 0.00184 0.00245 0.00979 * 0.01958 * 0.03917 * 0.07834 * 0.15667 *	10.000 10.000 10.000 10.000 10.00034 10.001208 10.001208 10.001461 10.001461 10.001461 10.00180 10.040182 10.080367 10.080367 10.16084	Pass/Fail
1000000000000 * Tolerance on output volume Ep 2: Actual Position (API) MSB LSB 00000000000000 00000000000000 000000	00000000000000000000000000000000000000	ARI Output Voltage Required (Vac) 0.00000 0.00061 0.00122 0.00184 0.00245 0.00490 * 0.00979 * 0.01958 * 0.03917 * 0.07834 * 0.15667 * 0.31334 *	10.000 10.000 10.000 10.000 10.000 10.00034 10.001208 10.001208 10.001461 10.004911 10.0034 10.040182 10.080367 10.16084 10.72168	Pass/Fail
10000000000000000000000000000000000000	00000000000000000000000000000000000000	ARI Output Voltage Required (Vgc)/ 0.00000 0.00061 0.00122 0.00184 0.00245 0.00490 * 0.00979 * 0.01958 * 0.03917 * 0.07834 * 0.15667 * 0.31334 * 0.62669 *	10.000 10.000 10.000 10.000 10.000 10.00034 10.001208 10.00	Pass/Fail
10000000000000000000000000000000000000	00000000000000000000000000000000000000	ARI Output Voltage Required (Vgc) 0.00000 0.00061 0.00122 0.00184 0.00245 0.00490 * 0.00979 * 0.01958 * 0.07834 * 0.15667 * 0.31334 * 0.62669 * 1.25338 *	10.000 10.000 10.000 10.000 10.000 10.00034 10.001208 10.001461 10.002461 10.002461 10.00034 10.00036 10.040182 10.080367 10.06034 10.080367 10.16084 10.32168 10.64347 11.2363	Pass/Fail
10000000000000000000000000000000000000	00000000000000000000000000000000000000	ARI Output Voltage Required (Vgc)/ 0.00000 0.00061 0.00122 0.00184 0.00245 0.00490 * 0.00979 * 0.01958 * 0.03917 * 0.07834 * 0.15667 * 0.31334 * 0.62669 *	10.000 10.000 10.000 10.000 10.000 10.00034 10.001208 10.00	Pass/Fail

TEST DATA SHEET B-13 (Sheet 3 of 3)

INTERFACE/CONVERTER CCA (P/N 1331697) (Paragraph 6.13.7)

6.13.7.5 Strobe F	unction		
Step 1: Strobe Lo	<u>w</u>	Pass/Fail	
No E11 Chang		<u></u>	
with Input CP	Changes		
Step 2: Strobe Hi	<u>gh</u>	- ·	
E11 Change		Pass/Fail	
with Input CP	Changes		
6.13.7.6 <u>Amplifie</u>	r Gain		
0.13.7.0 Ampinte		<u>Limits (Vdc) Pass/Fail</u>	
E11	Measured Value (Vdc) C. 321(7	Emins (voc) Fass/Fan	
E10	3.5464	<u> </u>	
E10 Voltage	11.0	10.7 - 11.3 P	
Ell Voltage			
6.13.7.7 <u>Ground I</u>	solation		
	Measured Value (MΩ)	Limits (MΩ) Pass/Fail	•
Pin 91 to Pin 7 DC Resistance		>20	
DC Resistance	taiger mailing		
_			
Comments:			
	n	plalea	
Conducted by:	Test Engineer	$\frac{8/7/97}{Date}$	
Verified by:	1 1 TA 190	C CT 10 '97	
vermed by.	Quality Control Inspector	Date	
Approved by:	Lucial Gramer	19/4/97 Date	
	DCMC	Date	

TEST DATA SHEET B-13 (Sheet I of 3)

INTERFACE/CONVERTER CCA (P/N 1331697) (Paragraph 6.13.7)

Date: 8/21/97 CCA S/N: F34 133/697-1

6.13.7.1 Supply Voltages

Supply	Measured Value (Vdc)	Limits (Vdc)	Pass/Fail
+5V (U)	5.01	+5V± 0.05	P
+15V (I)	15.01	+15V± 0.15	
-15V (I)	-14.97	-15V± 0.15	-
+5V (I)	5.02	+5V± 0.05	l P

6.13.7.2 Supply Currents

Step 1 (CP and API Low):

Supply	Measured Value (mA)	Limits (mA)	Pass/Fail
+5V (U)	26.45	70 - 110	
+5V (I)	3.34	1.5 - 5.5	P
+15V (I)	18.01	15 - 23	P
-15V (I)	20.71	18 - 26	l P

Step 2 (CP and API High):

Supply	Measured Value (mA)	Limits (mA)	Pass/Fail
+5V (U)	57.50	40 - 70	P
+5V (I)	23.90	18 - 30	J P
+15V (I)	18.01	15 - 23	P
-15V (I)	20.71	18 - 26	P

6.13.7.3 Amplifier Offsets

Γ	Amplifier	Measured Value (mV)	Limits (mV)	Pass/Fail
	AR1	-0.68	0.0 ±0.15	ſ
T	AR2	-0.06	0.0 ±2.0	ι ρ

TEST DATA SHEET B-13 (Sheet 2 of 3)

INTERFACE/CONVERTER CCA (P/N 1331697) (Paragraph 6.13.7)

		/.	£0.000	550
Actual Position (API)	Command Position (CP)	AR1 Output	Test Result	
MSB LSB	MSB LSB	Voltage Required (Vdc)	(Vdc)	Pass/Fa
0000000000000	00000000000000	0.00000	-0.000085	P
0000000000001	00000000000000	-0.00061	-0.00638	
000000000000000010	00000000000000	-0.00122 \	-0.coi272	,
0000000000011	000000000000000	-0.00184	-0.001910	1
00000000000100	00000000000000	-0.00245	-0.0c 2543	
0000000001000	00000000000000	-0.00490 ★	-0.00 5062	Ţ
0000000010000	000000000000000	-0.00979 ★	-0.016103	
0000000100000	00000000000000	-0.01958 *	-0. c202co	
0000001000000	00000000000000	-0.03917 ★	-0403 17	
00000010000000	. 000000000000000	-0.07834 ≯	-0.086763	<u>P</u>
00000100000000	00000000000000	-0.15667 ≯	-0.16150	
00001000000000	0000000000000	-0.31334 ★	-0.32301	<u></u> <u></u>
0001000000000	00000000000000	-0.62669 🛧	-0.64610	<u>_</u>
0010000000000	00000000000000	-1.25338 🛧	-1.2924	f
01000000000000	0000000000000	-2.50675 🛧	-2.5847	<u> </u>
10000000000000	00000000000000	-5.01350 * unifumae 9-10-97	10.000 ± 0.000 ± 0.000	60
100000000000000 Folerance on output vol	00000000000000000000000000000000000000	-5.01350 * unfumme 9-10-97	1 0.000	60
100000000000000 Folerance on output vol Actual Position (API)	00000000000000000000000000000000000000	-5.01350 * 27 / 9-10-97 ARI Output	10.000 ± 0.000 ± 0.000 Test Result (Vdc)	60 30
100000000000000 Folerance on output vol Actual Position (API) MSB LSB	00000000000000000000000000000000000000	-5.01350 * unfumme 9-10-97	10.000 ± 0.000 ± 0.000 Test Result (Vdc) - 0.66083	60 30
10000000000000 Folerance on output vol Actual Position (API) MSB LSB 00000000000000000000	00000000000000000000000000000000000000	-5.01350 * 4	10.000 ± 0.000 ± 0.000 Test Result (Vdc)	60 30
100000000000000 Folerance on output vol Actual Position (API) MSB LSB 00000000000000000000000000000000000	00000000000000000000000000000000000000	-5.01350 * -5.01350 * -5.01350 * AR1 Output Voltage Required (Vgc)/ 0.00000	10.000 10.000 10.000 10.000 10.000 10.000 10.000 10.000 10.000 10.000 10.000 10.000	60 30
10000000000000 Folerance on output vol Actual Position (API) MSB LSB 0000000000000000000 00000000000000	00000000000000000000000000000000000000	-5.01350 * -5.01350 * 9-10-97 AR1 Output Voltage Required (Vac) 0.00000 0.00061	10.000 10.000 10.000 10.000 10.000 10.000 10.000 10.001 10.001 10.001 10.001 10.001 10.001 10.001	60
100000000000000 Folerance on output vol Actual Position (API) MSB LSB 0000000000000000 00000000000000000	00000000000000000000000000000000000000	-5.01350 * 9-10-97 AR1 Output* Voltage Required (Vgc)/ 0.00000 0.00061 0.00122	10.000 10.000 10.000 10.000 10.000 10.0016 10.001794 10.002424	Pass/Fa
100000000000000 Folerance on output vol Actual Position (API) MSB LSB 0000000000000000 00000000000000000	00000000000000000000000000000000000000	-5.01350 * 9-10-97 ARI Output Voltage Required (Vgc)/ 0.00000 0.00061 0.00122 0.00184	10.000 10.000 10.000 10.000 10.000 10.00536 10.001168 10.001794 10.001794 10.001794	60 30
100000000000000 Folerance on output vol Actual Position (API) MSB LSB 00000000000000 00000000000000 00000000	00000000000000000000000000000000000000	-5.01350 * Wy furm 0 9-10-97 AR1 Output Voltage Required (Vac) 0.00000 0.00061 0.00122 0.00184 0.00245	10.000 10.000 10.000 10.000 10.000 10.000 10.00169 10.001794 10.001424 10.001424 10.004943 10.0010020	Pass/Fa
100000000000000 Folerance on output vol Actual Position (API) MSB LSB 000000000000000 000000000000000 0000	00000000000000000000000000000000000000	-5.01350 * -5.01350 * 9-10-97 AR1 Output Voltage Required (Vac) 0.00000 0.00061 0.00122 0.00184 0.00245 0.00490 *	10.000 10.000 10.000 10.000 10.00083 10.00168 10.001794 10.001794 10.001794 10.001794 10.001794 10.001794	Pass/Fa
1000000000000000 Folerance on output vol Actual Position (API) MSB LSB 00000000000000 00000000000000 00000000	00000000000000000000000000000000000000	-5.01350 * -5.01350 * -5.01350 * -5.01350 * AR1 Output* Voltage Required (Vgc)/ 0.00000 0.00061 0.00122 0.00184 0.00245 0.00490 * 0.00979 *	10.000 10.000 10.000 10.000 10.000 10.000 10.00169 10.001794 10.001424 10.001424 10.004943 10.0010020	Pass/Fa
1000000000000000 Folerance on output vol Actual Position (API) MSB LSB 000000000000000 000000000000000 0000	00000000000000000000000000000000000000	-5.01350 * 9-10-97 ARI Output Voltage Required (Vgc) 0.00000 0.00122 0.00184 0.00245 0.00490 * 0.00979 * 0.01958 *	10.000 10.000 10.000 10.000 10.00083 10.00168 10.001794 10.001794 10.001794 10.001794 10.001794 10.001794	Pass/Fa
10000000000000000 Folerance on output vol Actual Position (API) MSB LSB 000000000000000 00000000000000 0000000	00000000000000000000000000000000000000	-5.01350 * -5.01350 * 9-10-97 AR1 Output Voltage Required (Vac) 0.00000 0.00061 0.00122 0.00184 0.00245 0.00490 * 0.00979 * 0.01958 * 0.03917 *	10.000 10.000 10.000 10.000 10.000 10.000 10.00168 10.001794 10.001794 10.001794 10.001794 10.001794 10.001794 10.001794 10.001794 10.001794 10.001794	Pass/Fa
100000000000000 Folerance on output vol Actual Position (API) MSB LSB 000000000000000 00000000000000 00000	00000000000000000000000000000000000000	-5.01350 * -5.01350 * -5.01350 * AR1 Output Voltage Required (Vyc)/ 0.00000 0.00061 0.00122 0.00184 0.00245 0.00490 * 0.00979 * 0.01958 * 0.03917 * 0.07834 *	10.000 10.000 10.000 10.000 10.000 10.00083 10.00168 10.001794 10.001794 10.001474 10.0014943 10.0010020 10.0010020 10.0010020 10.00105 10.01015 10.01015 10.01015 10.01015 10.01015 10.01015 10.01015 10.01015 10.01015 10.01015 10.01015	Pass/Fa
10000000000000 Tolerance on output vol Actual Position (API) MSB LSB 00000000000000 0000000000000 00000000	00000000000000000000000000000000000000	-5.01350 * -5.01350 * -5.01350 * AR1 Output* Voltage Required (Vgc)/ 0.00000 0.00061 0.00122 0.00184 0.00245 0.00490 * 0.00979 * 0.01958 * 0.03917 * 0.07834 * 0.15667 *	10.000 10.000 10.000 10.000 10.00083 10.00168 10.001794 10.001794 10.001424 10.0014943 10.0016020 10.0040302 10.080615 10.16148 10.32305 10.64627	Pass/F2 P P P P P P P P P
100000000000000 Folerance on output vol Actual Position (API) MSB LSB 000000000000000 00000000000000 00000	00000000000000000000000000000000000000	-5.01350 * -5.01350 * -5.01350 * AR1 Output Voltage Required (Vgc)/ 0.00000 0.00061 0.00122 0.00184 0.00245 0.00490 * 0.00979 * 0.01958 * 0.03917 * 0.07834 * 0.15667 * 0.31334 *	10.000 10.000 10.000 10.000 10.00083 10.001794 10.001794 10.001794 10.001794 10.001943 10.0016020 10.0016020 10.0016020 10.0016 10.040302 10.080615 10.16148 10.32305 10.64627 11.2921	Pass/F2 P P P P P P P P P
10000000000000 Folerance on output vol Actual Position (API) MSB LSB 000000000000000 00000000000000 00000	00000000000000000000000000000000000000	-5.01350 * One of the second	10.000 10.000 10.000 10.000 10.00083 10.00168 10.001794 10.001794 10.001424 10.0014943 10.0016020 10.0040302 10.080615 10.16148 10.32305 10.64627	Pass/Fa

TEST DATA SHEET B-13 (Sheet 3 of 3)

INTERFACE/CONVERTER CCA (P/N 1331697) (Paragraph 6.13.7)

6.13.7.5 Strobe	Function		
0.15.7.5 <u>Subbe</u>	<u>-unction</u>		
Step 1: Strobe Lo	<u>ow</u>	·	
No EII Chan	ITA	Pass/Fail .	
with Input CF			
Step 2: Strobe H	igh	Pass/Fail	
E11 Change		Passiran P	
with Input CP	Changes		
61276 AUE-	` 		
6.13.7.6 <u>Amplifie</u>	er Gain		
	Measured Value (Vdc)	Limits (Vdc) Pass/Fail	
E11	0.32306		
E10	3.5664		. •
E10 Voltage	11.04	10.7 - 11.3	
El I Voltage			
6.13.7.7 <u>Ground I</u>	solation		
		Tivin A(O) D F II	•
Pin 91 to Pin 7	Measured Value (M Ω)	Limits (MΩ) Pass/Fail	
DC Resistance	7 150MN	>20	
	,	•	
Comments:	4.5		
No	NE		
Conducted by:	Derne Lun	8/21/91 -	
conducted by.	Test Engineer	Date	
	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	OCT 19 '97	
Verified by:			
	Quality Control Inspector	Date (2)	•
Approved by:	Cubul Shines	11/14/19/	
	DCMC '	Date	

TEST DATA SHEET B-4 (Sheet 1 of 2)

MOTOR DRIVER 3-HALL SENSOR CCA (P/N 1331694) (Paragraph 6.4.3)

S/N:

F#4

Date:

8/21/97

6.4.3.2 Input Signal Offset

4 1.769 mV 0.0 ±1 mVdc 6 1.372 mV 0.0 ±1 mVdc	Coop No	Test Results	Limits
0 1 1. 2/ V MV	Step No.	1 7/9 mV	0.0 ±1 mVdc
		1 372 101/	0.0 ±1 mVdc
0 1 1 1 1 1 0.0 ±1 11 1 4 0 0		1513 41	0.0 ±1 mVdc

Step No.	Test Resistor	Resistance Measured
13	E7-E8 (R25)	3-16K
13	E9-E10 (R52)	6.041
•	E11-E12 (R33)	2.80 K
	E13-E14 (R53)	4.22K
	E15-E16 (R42)	3.16K
	E17-E18 (R54)	5.23 K

Step No.	Resistors	Selected Trim Resistors
14	R25	RNC 5553161FS
17 F	R52	RNC55J6041FS
-	R33	RNC55J2801FS
-	R53	RNC55J4221FS
<u> </u>	R42	RNC 55 J 3161 FS
-	R54	RNC 55 J 523 IFS

	E Point	Test Results	Limits	Pass/Fail
Step No.	E Foint	-0.038 hV	0.0 ±1 mVdc	PASS
19	E20	10.020 mV	0.0 ±1 mVdc	PASS
ļ-	E20	- 0.015 mV	0.0 ±1 mVdc	PASS

6.4.3.3 Motor Driver Operation

Clockwise Rotation:

Step No.	Test Results	Limits	Pass/Fail
2	5.01V	+5V±0.05Vdc	PASS
-	52.6NA	70mAdc max	PASS
<u> </u>	15.00	+15V±0.15Vdc	PASS
-	1.5 m/	3.0mAdc max	PASS
·	-14.97V	-15V±0.15Vdc	PASS
·	18.44mA	25mAdc max	PASS
	28.0V	+28V±0.5Vdc	FASS
. F	5.6MA	8mAdc max	PASS
3	280 mV	400mVdc max	PASS
4	40 MA	50mAdc max	PASS
5	48 m/	50mAdc max	I PASS



TEST DATA SHEET B-4 (Sheet 2 of 2)

MOTOR DRIVER 3-HALL SENSOR CCA (P/N 1331694) (Paragraph 6.4.3)

Counter Clockwise Rotation:

Step No.	Test Results	Limits	Pass/Fail
3tep 140.	271 MV	400mVdc max	PASS
1 - 3	36 MA	50mAdc max	PASS
	40 mA	50mAdc max	PASS

6.4.3.4 Current Limit Test

Step No.	Test Results	Limits	Pass/Fail
3	450 MA	350-500mAdc	PASS

Comments:	JONE
	·
	••
_	
	Danit 2 1/2/97
Conducted by:	Test Engineer Date
Verified by:	Judie Jensey (%) 09/03/97
	Otality Control Inspector Date
Approved by:	DCMC Date

TEST DATA SHEET B-4 (Sheet 1 of 2)

MOTOR DRIVER 3-HALL SENSOR CCA (P/N 1331694) (Paragraph 6.4.3)

S/N:

FII

Date:

8/21/97 1331694-3

6.4.3.2 Input Signal Offset

Step No.	Test Results	Limits
Step 140.	+1.02 mV	0.0 ±1 mVdc
4	+0.65 mV	0.0 ±1 mVdc
6		0.0 ±1 mVdc
8	+1.03 mV	0.0 21 111 100

Step No.	Test Resistor	Resistance Measured
13	E7-E8 (R25)	4.22K
13	E9-E10 (R52)	6.04K
	E11-E12 (R33)	N/A
,	E13-E14 (R53)	~/A
	E15-E16 (R42)	3.74 K
	E17-E18 (R54)	5.62k

Step No.	Resistors	Selected Trim Resistors
14	R25	RNCSS J4221FS
17	R52	RNC5576041FS
-	R33	NIA
<u> </u>	R53	N/A
	R42	RNC 55 J 3741FS
	R54	RNC55 J 5621 FS

	E D-:	Test Results	Limits	Pass/Fail
Step No.	E Point		0.0 ±1 mVdc	PASS
19	E19	10.014 my		PASS
	E20	+0.649 mV	0.0 ±1 mVdc	
	E21	-0.063 mV	0.0 ±1 mVdc	1 PASS

6.4.3.3 Motor Driver Operation

Clockwise Rotation:

Step No.	Test Results	Limits	Pass/Fail
2 Step No.	5.017	+5V±0.05Vdc	PASS
	52.48mA	70mAdc max	PASS
<u> </u>	15.0cV	+15V±0.15Vdc	PASS
<u> </u>	1.53 mA	3.0mAdc max	PASS
<u> </u>	-14.97V	-15V±0.15Vdc	PASS
·	18.37 MA	25mAdc max	PASS
-	28.00 V	+28V±0.5Vdc	PASS
	5. 61 mA	8mAdc max	PASS
	270hV	400mVdc max	PASS
4	41 MA	50mAdc max	PASS
5	471111	50mAdc max	PASS

TEST DATA SHEET B-4 (Sheet 2 of 2)

MOTOR DRIVER 3-HALL SENSOR CCA (P/N 1331694) (Paragraph 6.4.3)

Counter Clockwise Rotation:

Step No.	Test Results	Limits	Pass/Fail
3	7.30 MV	400mVdc max	PASS
- 1	35mA	50mAdc max	'(ASS
	HOMA	50mAdc max	PASS

6.4.3.4 Current Limit Test

Step No.	Test Results	Limits	Pass/Fail
3	450 MA	350-500mAdc	MSS

Comments:	···			
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Conducted by:	Test Engineer	8/21/97 Date	-	
Verified by:	Quality Control Inspector	3) <u>09/03/97</u> Date		
Approved by:	DCMC Stomes	<u>9/3/97</u> Date		

TEST DATA SHEET B-5 (Sheet 1 of 3)

R-D CONVERTER/OSCILLATOR CCA (P/N 1337739) (Paragraph 6.5.7)

Date 4/14/98 CCA S/N = 22

6.5.7.1 <u>UUT Pre-Test</u>

Step 2:

Supply Currents (Without UUT)

Supply (Vdc)	(Baseline) Measured Value (mA) (Without UUT)	Limits (mA)	Pass/Fail
+15	0.06	0-1	P
-15	-0.28	-1 - 0	P
+5 \	0.06	0-1	P

Supply Voltages (Without UUT)

Supply	Measured Value (V)	Limits (V)	Pass/Fail
+15V (I)	15.018	± 0.50	P
-15V (I)	-15.016	± 0.50	ρ
-15V (I)	5.033	±0.25	P
+3V(I)			

Step 6:

Supply Currents (UUT Installed)

Measured Value (mA)	Difference (mA) (Measured - Baseline)	Limits (mA)	Pass/Fail
	27.75	20-40	P
	-37.19	-3050	P
	62.82	30-70	P
	Measured Value (mA) (UUT Installed) 27.8/ -37.47 62.88	(UUT Installed) (Measured - Baseline) 27.81 27.75 -37.47 -37./9	(UUT Installed) (Measured - Baseline) 27.8/ 27.75 20-40 -37.47 -37./9 -3050

6.5.7.2 Supply Voltages (UUT Installed)

Measured Value (V)	Limits (V)	Pass/Fail
	± 0.50	P
-14.973	± 0.50	P
5.018	±0.25	P
	Measured Value (V) /5.0/2 -/4.973 5.0/8	/5.0/2 ± 0.50 -/4.973 ± 0.50

6.5.7.3 Oscillator Frequency, Duty Cycle, and Output Voltage

Parameter	Measured Value	Limits	Pass/Fail
Frequency	1613.6	1550-1650 Hz	P
Duty Cycle	51.41	45-55 %	P
Output Voltage	8.147	7.6-8.4 Vrms	P

TEST DATA SHEET B-5 (Sheet 2 of 3)

R-D CONVERTER/OSCILLATOR CCA (P/N 1337739) (Paragraph 6.5.7)

R-D Converter Operation 6.5.7.4

Step 1:

Bit Number/	CW	CCW
Test Fixture Label	Pass/Fail	Pass/Fail
API 0/1	P	P
API 1/2	Ρ	P
API 2/3	ρ	β
API 3/4	P	Р
API 4/5	P	P
API 5/6	P	P
API 6/7	Ρ	P
API 7/8	P	P
API 8/9	P	P
API 9/10	P	Ρ
API 10/11	ρ	P
API 11/12	P	P
API 12/13	Р	P
API 13/14	<i>P</i>	Ρ
Converter Busy		م

Step 2:

RS Œ10)	Measured Value (Vdc)	Calculated Value (Vdc) * CCA -1 Assy	Calculated Value (Vdc) * CCA -2 Assy	Pass/Fail
CW Rotation	1.78	(+) 1.789	(+) NA	P
CCW Rotation	- 1815	(-) - 1.789	(-) NA	P
CCW ROLLION	7,0,0	<u> </u>		1/

* Signal level function of test and calibration gain resistors. Record calculated value and measured value. Measured value shall be within ± 20 percent of calculated value. The equation is as follows: $V = \pm 0.155 \left(\frac{R20}{R17}\right) \pm 20\%$

$$V = \pm 0.155 \left(\frac{R20}{R17} \right) \pm 209$$

Amplifier Gain 6.5.7.5

Measured Value (Vdc)	Limits (Vdc)	Pass/Fail
1.105	1.00 to 1.30	P
1.135	1.00 to 1.30	P
	(Vdc)	(Vdc) 1.105 1.00 to 1.30

6.5.7.6 Direction Control Signal

DIR CNTRL	Measured Value (Vdc)	Limits (Vdc)	Pass/Fail
CW Rotation	5.001	4.5 to 5.5	P
CCW Rotation	0./29	0.0 to 0.4	P

TEST DATA SHEET B-5 (Sheet 3 of 3)

R-D CONVERTER/OSCILLATOR CCA (P/N 1337739) (Paragraph 6.5.7)

6.5.7.7	Notch Filter Frequency Response
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Frequency	Measured Value (Hz)	Calculated Value (Hz) * CCA -1 Assy	Calculated Value (Hz) * CCA-2 Assy	Pass/Fail
AR3 Notch	NA	NA	NA	NA
AR4 Notch				
AR5 Notch		<u> </u>		

^{*} Notch frequencies shall be within ±3 percent of values determined by test and calibration resistors. Record calculated and measured values.

Comments:

LEVEL AS ALLOWED IN AE-26693 p. 53

Conducted by:

Test Engineer

Date

Verified by:

and Morgan

4/14/95

Approved by:

APR 13 '93

Date

TEST DATA SHEET B-5 (Sheet 1 of 3)

R-D CONVERTER/OSCILLATOR CCA (P/N 1337739) (Paragraph 6.5.7)

Date 4/14/98 CCA S/N F25

6.5.7.1 <u>UUT Pre-Test</u>

Step 2:

Supply Currents (Without UUT)

Supply (Vdc)	(Baseline) Measured Value (mA) (Without UUT)	Limits (mA)	Pass/Fail
+15	0.06	0-1	P
-15	- 0.28	-1 - 0	P
+5	0.06	0-1	P

Supply Voltages (Without UUT)

Supply	Measured Value (V)	Limits (V)	Pass/Fail
+15V (I)	15.018	± 0.50	P
-15V (I)	-15.016	± 0.50	P
+5V (I)	5.033	±0.25	ρ

Step 6:

Supply Currents (UUT Installed)

Supply (Vdc)	Measured Value (mA) (UUT Installed)	Difference (mA) (Measured - Baseline)	Limits (mA)	Pass/Fail
+15	3/.87	31.81	20-40	P
-15	-37.81	- 37.57	-3050	P
+5	55.3	55.24	30-70	P

6.5.7.2 Supply Voltages (UUT Installed)

Supply	Measured Value (V)	Limits (V)	Pass/Fail
+15V (I)	15.01	± 0.50	P
-15V (I)	-14.972	± 0.50	P
+5V (I)	5.019	±0.25	P

6.5.7.3 Oscillator Frequency, Duty Cycle, and Output Voltage

Parameter	Measured Value	Limits	Pass/Fail
Frequency	1630.17	1550-1650 Hz	P
Duty Cycle	51.26	45-55 <i>%</i>	P
Output Voltage	8.362	7.6-8.4 Vrms	P

TEST DATA SHEET B-5 (Sheet 2 of 3)

R-D CONVERTER/OSCILLATOR CCA (P/N 1337739) (Paragraph 6.5.7)

6.5.7.4 R-D Converter Operation

Step 1:

Bit Number/	CW	CCW
Test Fixture Label	Pass/Fail	Pass/Fail
API 0/1	P	P
API 1/2	P	Ρ.
API 2/3	P	P
API 3/4	Ρ	ρ
API 4/5	ρ	P
API 5/6	Р	ρ
API 6/7	P	P
API 7/8	ρ	P
API 8/9	P	P
API 9/10	Ρ	P
API 10/11	P	P
API 11/12	P	P
API 12/13	P	P
API 13/14	P	ρ
Converter Busy	ρ	P

Step 2:

RS (E10)	Measured Value (Vdc)	Calculated Value (Vdc) * CCA -1 Assy	Calculated Value (Vdc) * CCA -2 Assy	Pass/Fail
CW Rotation	1.753	(+) 1.789	(+) ~A	P
CCW Rotation	-1.812	(-) - 1.789	(-) NA	ρ

* Signal level function of test and calibration gain resistors. Record calculated value and measured value. Measured value shall be within ±20 percent of calculated value. The equation is as follows:

$$V = \pm 0.155 \left(\frac{R20}{R17} \right) \pm 20\%$$

6.5.7.5 Amplifier Gain

isa

PES-RS	Measured Value (Vdc)	Limits (Vdc)	Pass/Fail
PES = +0.300 Vdc	1.094	1.00 to 1.30	P
PES = -0.300 Vdc	1.154	1.00 to 1.30	م

6.5.7.6 Direction Control Signal

DIR CNTRL	Measured Value (Vdc)	Limits (Vdc)	Pass/Fail
CW Rotation	5.002	4.5 to 5.5	P
CCW Rotation	0.115	0.0 to 0.4	P

TEST DATA SHEET B-5 (Sheet 3 of 3)

R-D CONVERTER/OSCILLATOR CCA (P/N 1337739) (Paragraph 6.5.7)

6.5.7.7 Notch	Filter Frequency Response			
Frequency	Measured Value (Hz)	Calculated Value (Hz) * CCA -1 Assy	Calculated Value (Hz) * CCA-2 Assy	Pass/Fail
A DO Mosel	NA	NA	NA	NA
AR3 Notch AR4 Notch				1
AR5 Notch	1	<u> </u>	V	· · ·

^{*} Notch frequencies shall be within ±3 percent of values determined by test and calibration resistors. Record calculated and measured values.

Comments:

LEVEL AS ALLOWED IN
AE-26693 p. 53

Conducted by:

Test Engineer

Date

Verified by:

and Morgan

4/15/98

Quality Control Inspector

Date

Approved by:

APR 13 '98

Date

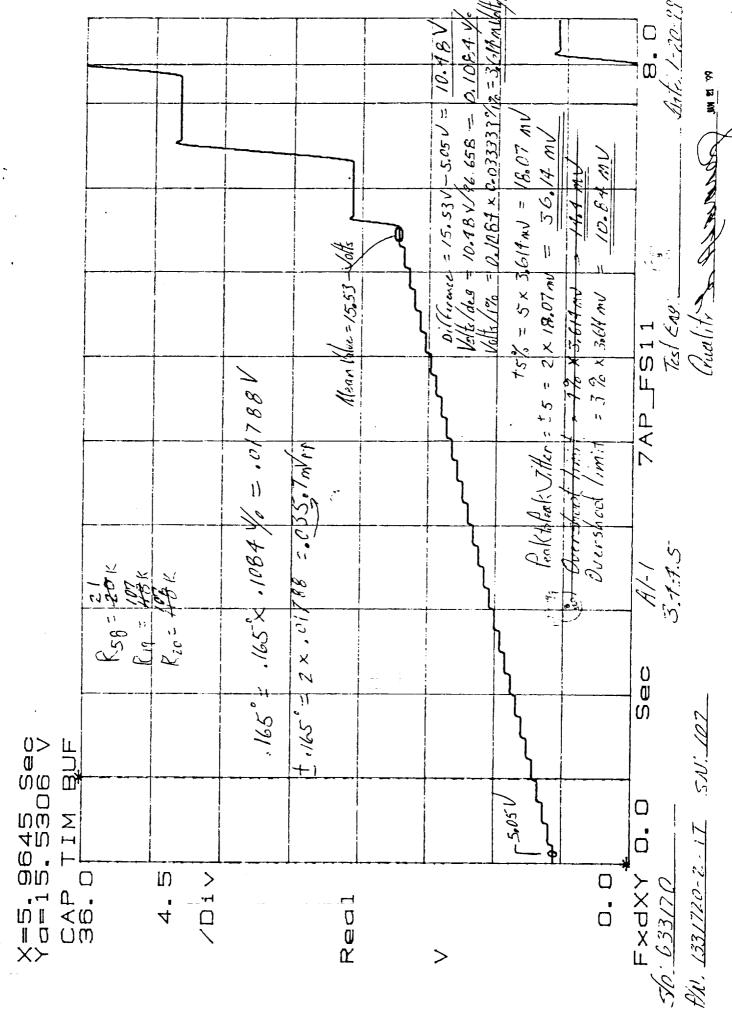
APPENDIX B SCAN MOTION AND JITTER RESPONSE PLOTS

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	MEASURE.	CHAN 1 Power Spe	Ú	CHAN 2	
	WINDOW.	CHAN 1 Hanning		CHAN Hanina Qui	
	AVERAGE.	TYPE Avg Off	# AVGS	OVERLAP O%	TIME AVG Off
	T REO.	CENTER 500 Hz		SPAN 1. OKIN	BW 1.87 Hz
		REC LGTH 800mS	Δt 391μS		
	TRIGGER.	TYPE External	LEVEL O.O VPK	SLOPE Neg	
	INPUT CH 1	RANGE AutoRng^ AutoRng^	ENG UNITS 1.0 V/EU 1.0 V/EU	COUPLING DC (Gnd)	DELAY 0.0 S 0.0 S
	SOURCE.	TYPE Off		LEVEL D. O VPK	0FFSET 0.0 Vpk
55	540: 053/70 811: 133/720-2-17	3.t.	45-78 Test Ens.	1. (1. (2. (1. (1. (1. (1. (1. (1. (1. (1. (1. (1	Into: 1-20-1

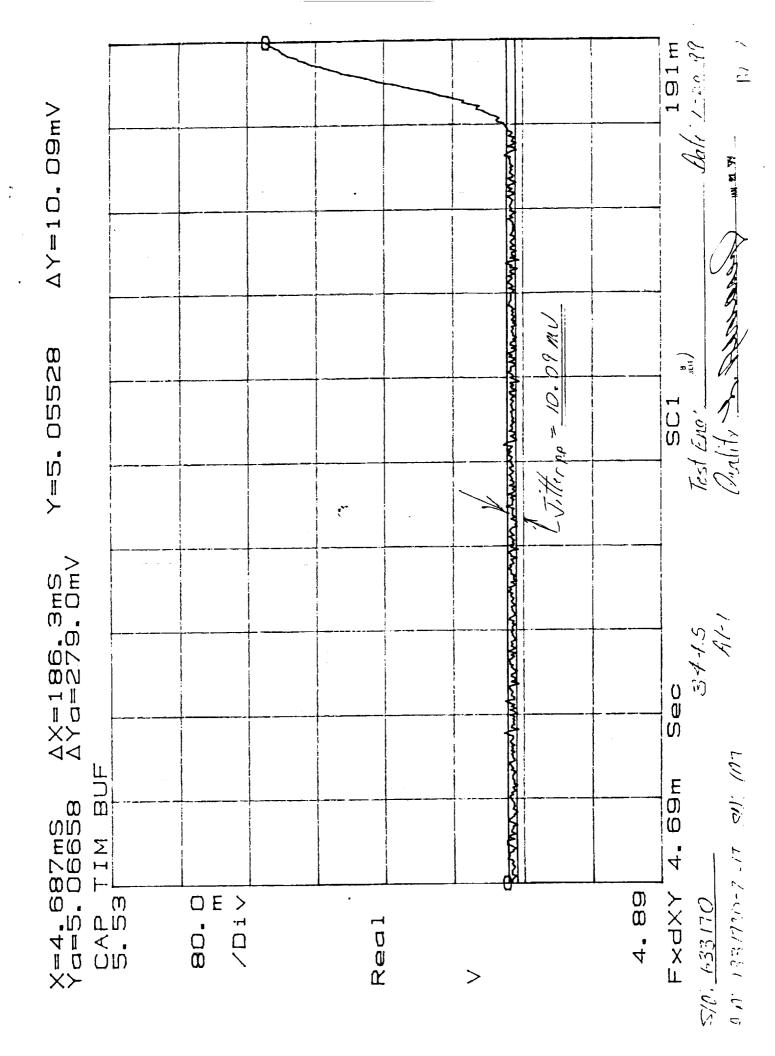
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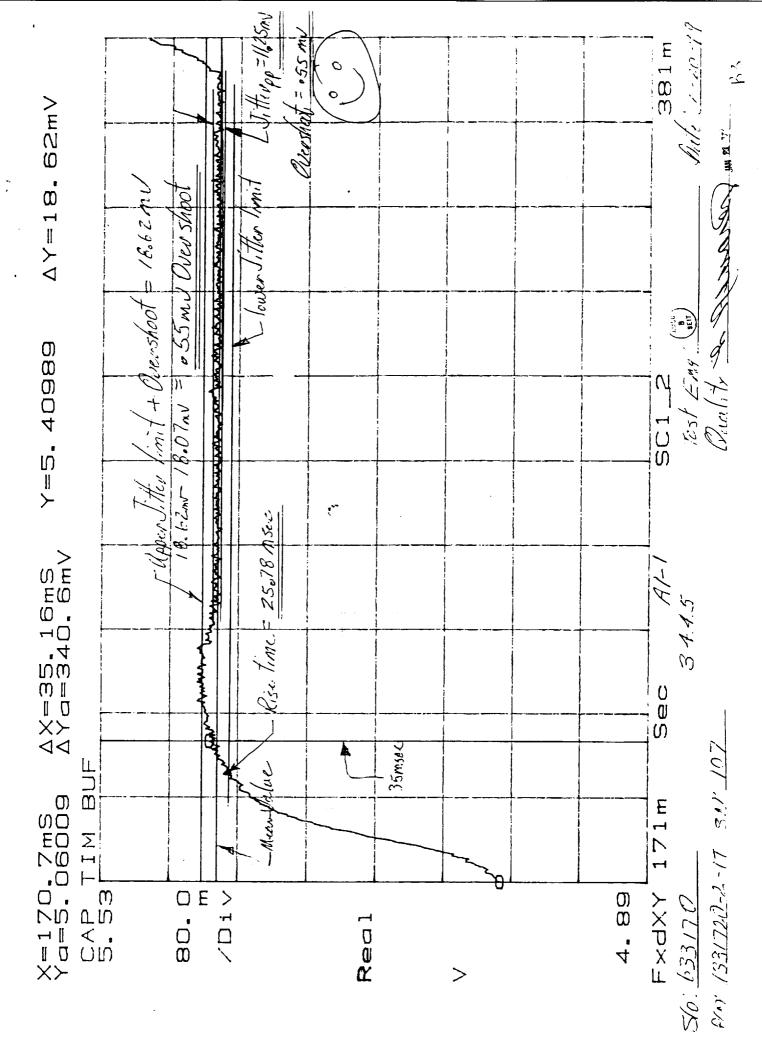
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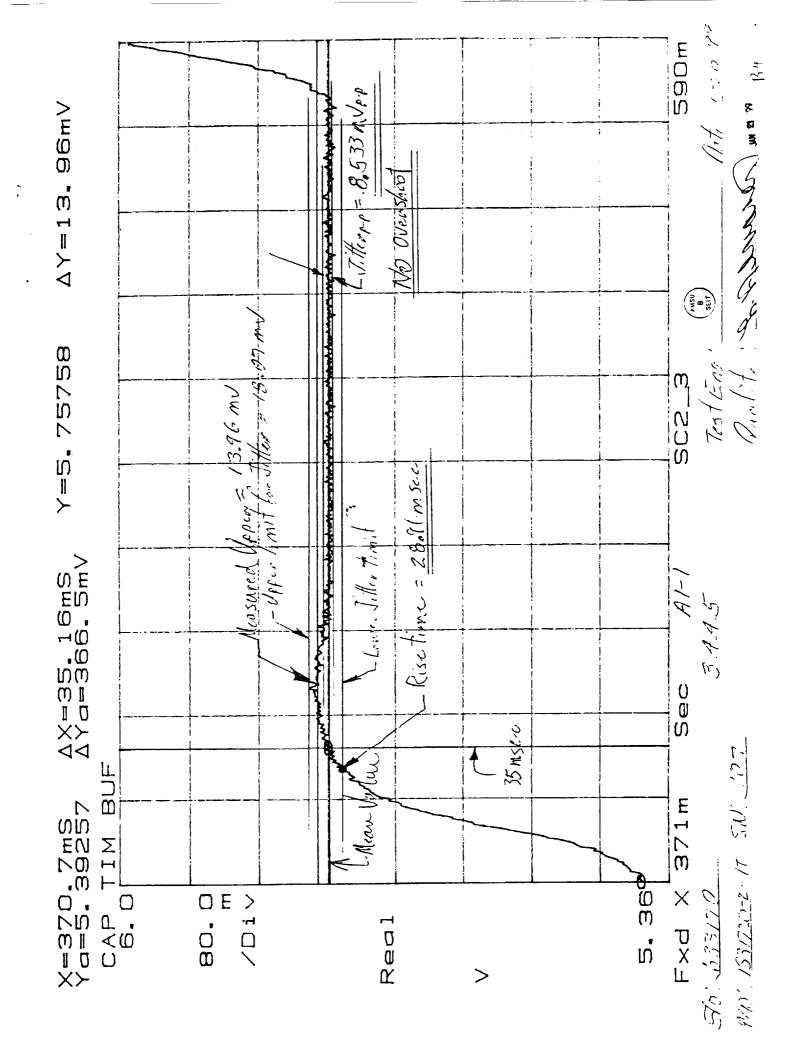


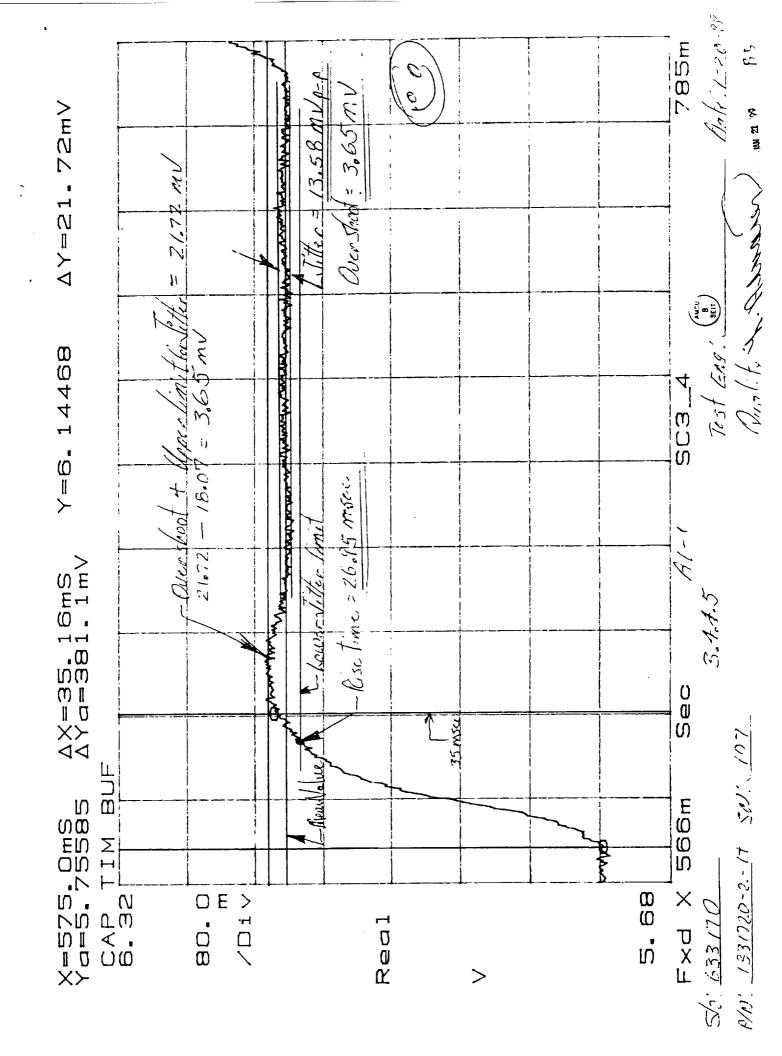
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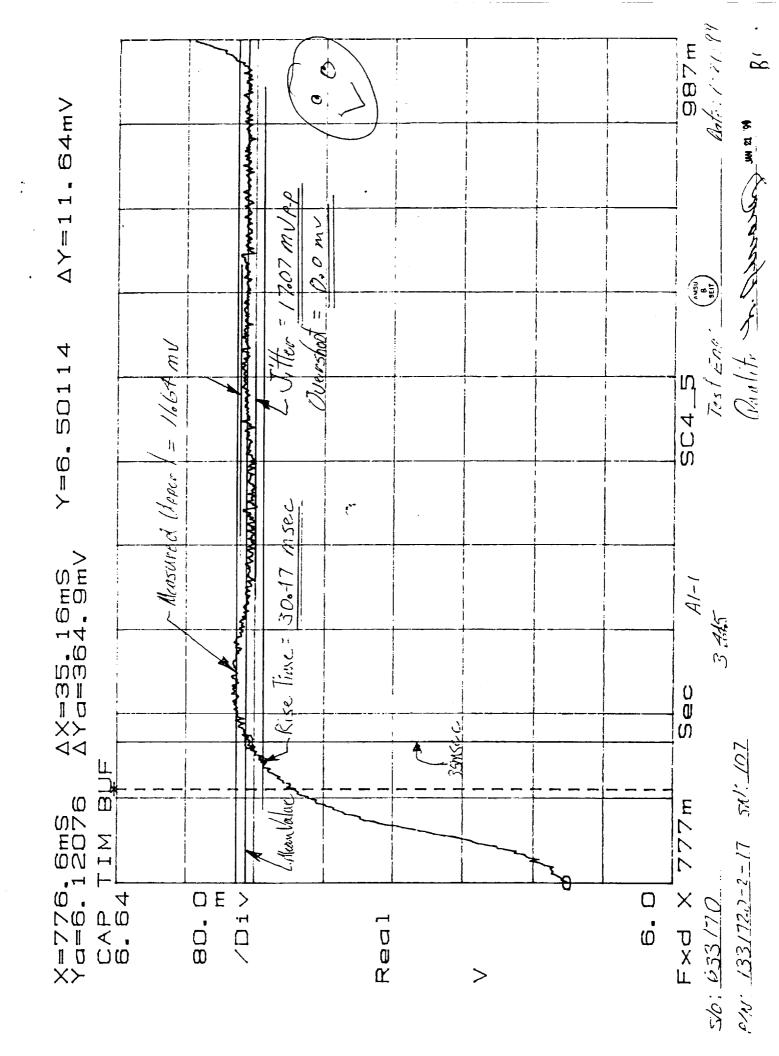
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MEASURE.	CHAN 1 Power Spec	O	CHAN 2 Off	•
WINDOW	CHAN 1 Hanning		CHAN N Haning	
AVERAGE.	TYPE Avg Off	# AVGS 10	OVERLAP O%	TIME AVG
FREO.	CENTER 500 Hz	ęw	SPAN 1. OKHZ	BW 1.87 Hz
	REC LGTH 800mS	Δt 391μS		
TRIGGER:	TYPE External	LEVEL O.O VPK	SLOPE Neg	
INPUH. CH 1	RANGE A∪toRng+ A∪toRng+	ENG UNITS 1.0 V/EU 1.0 V/EU	COUPLING DC (Gnd) DC (Gnd)	DELAY 0.0 S 0.0 S
SOURCE.	TYPE Off		LEVEL O.O VDA	OFFSET O.O Obk
40: 133/720-2-17 SN: 102		3.4.45-78 Test Ens.	(est Live: (me) (seri)	Arts: 1
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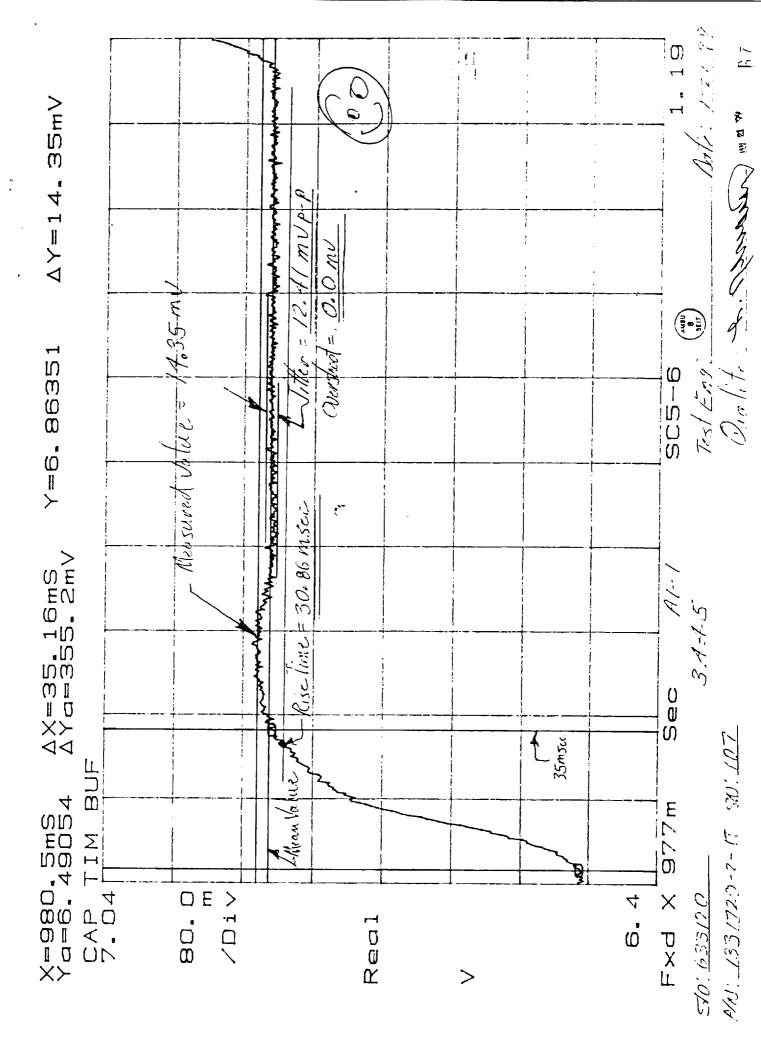


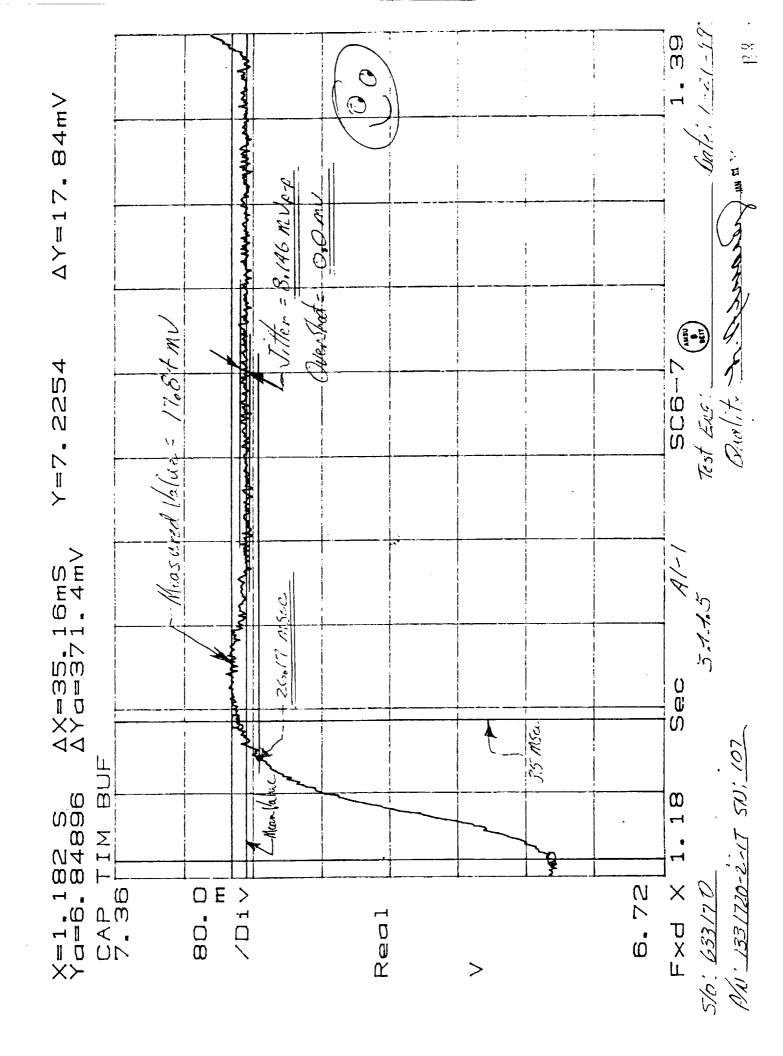


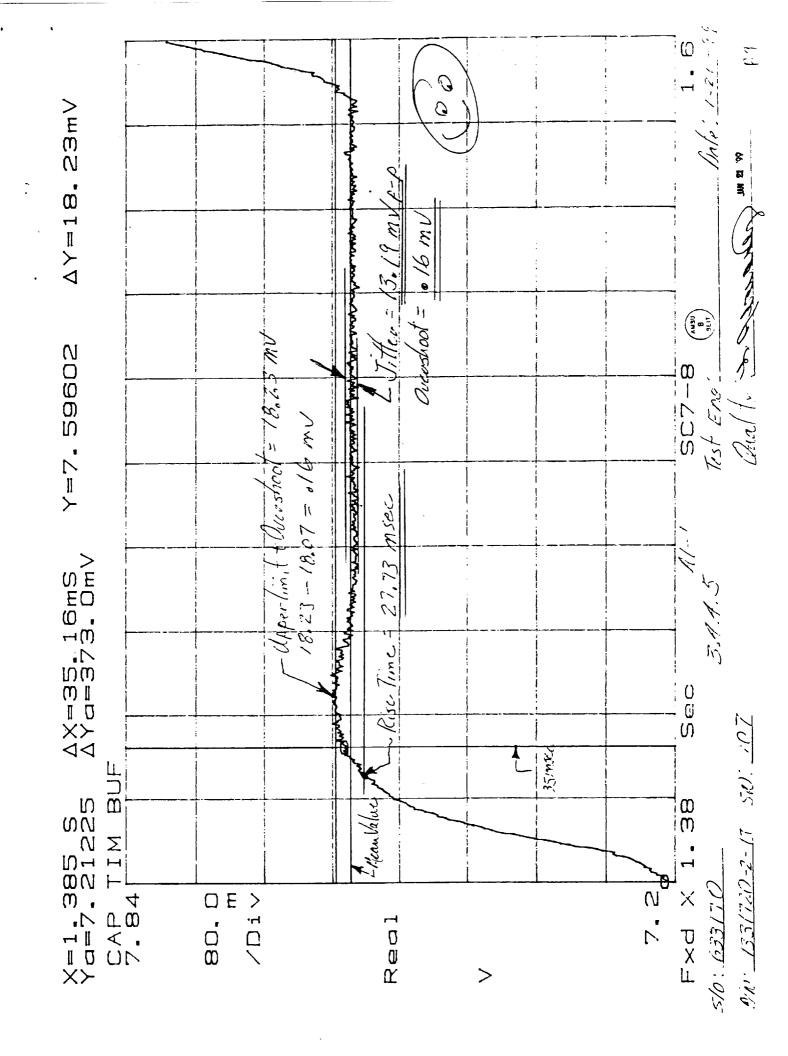


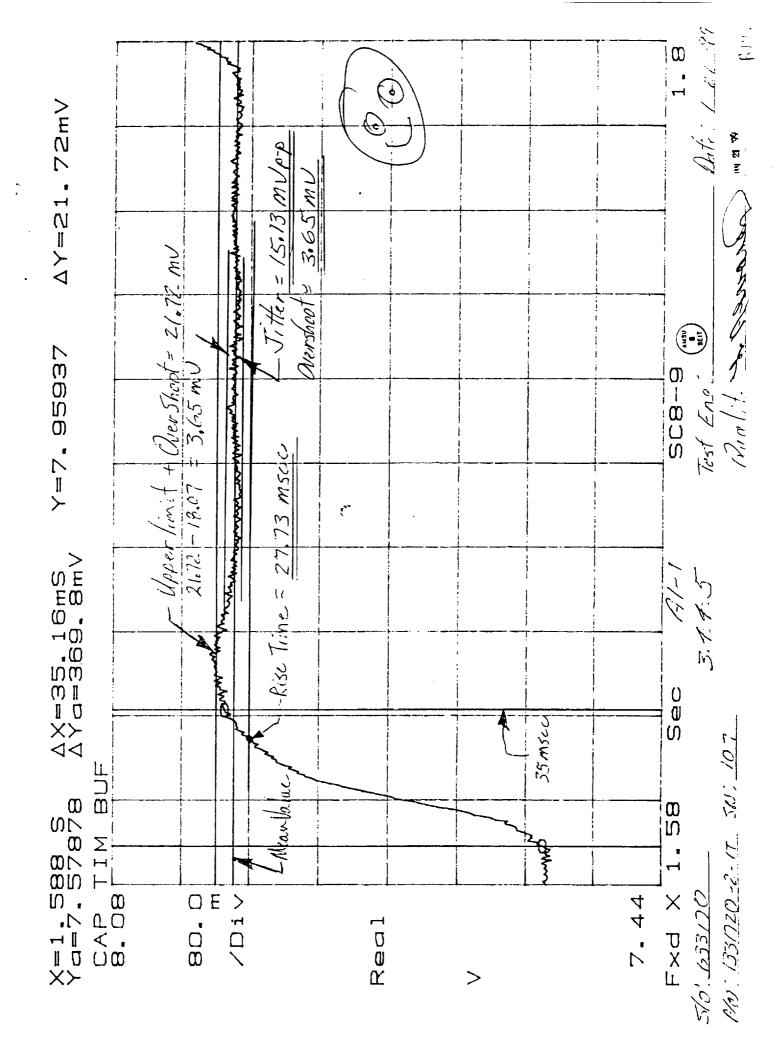


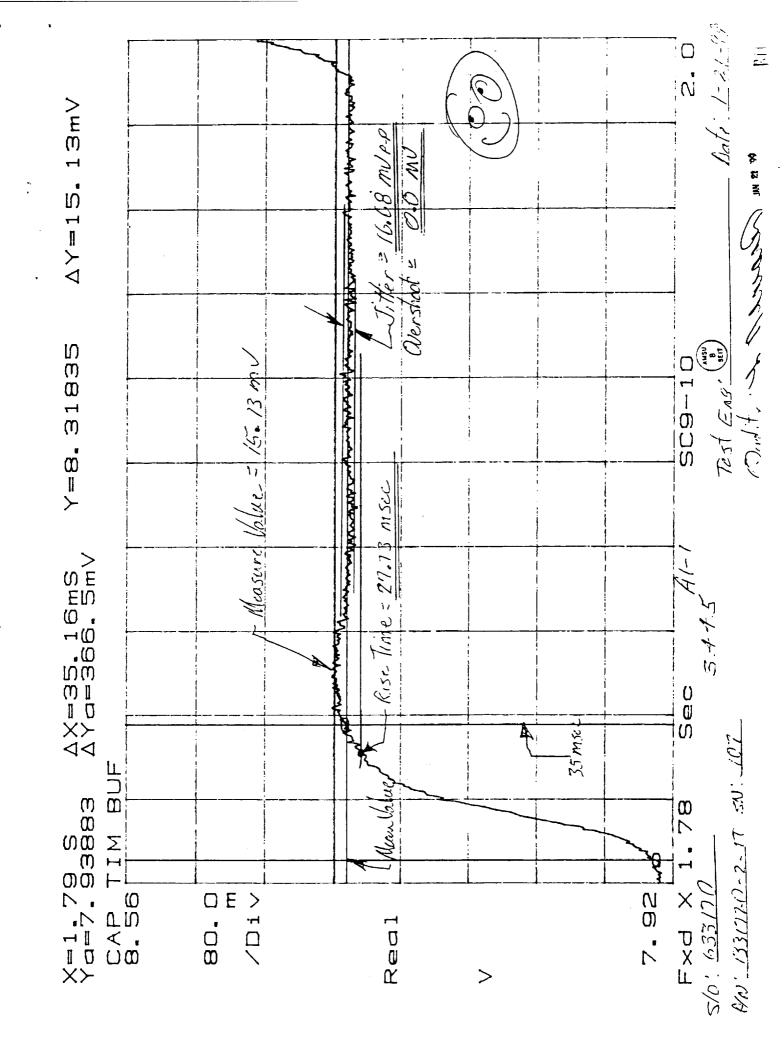


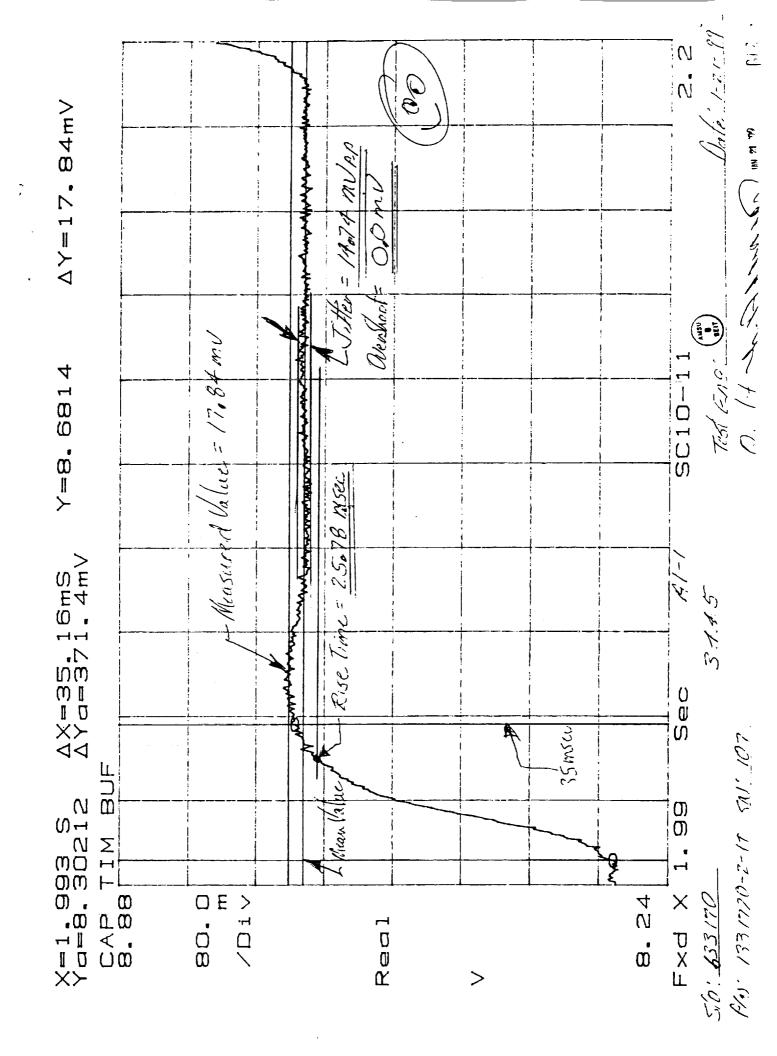


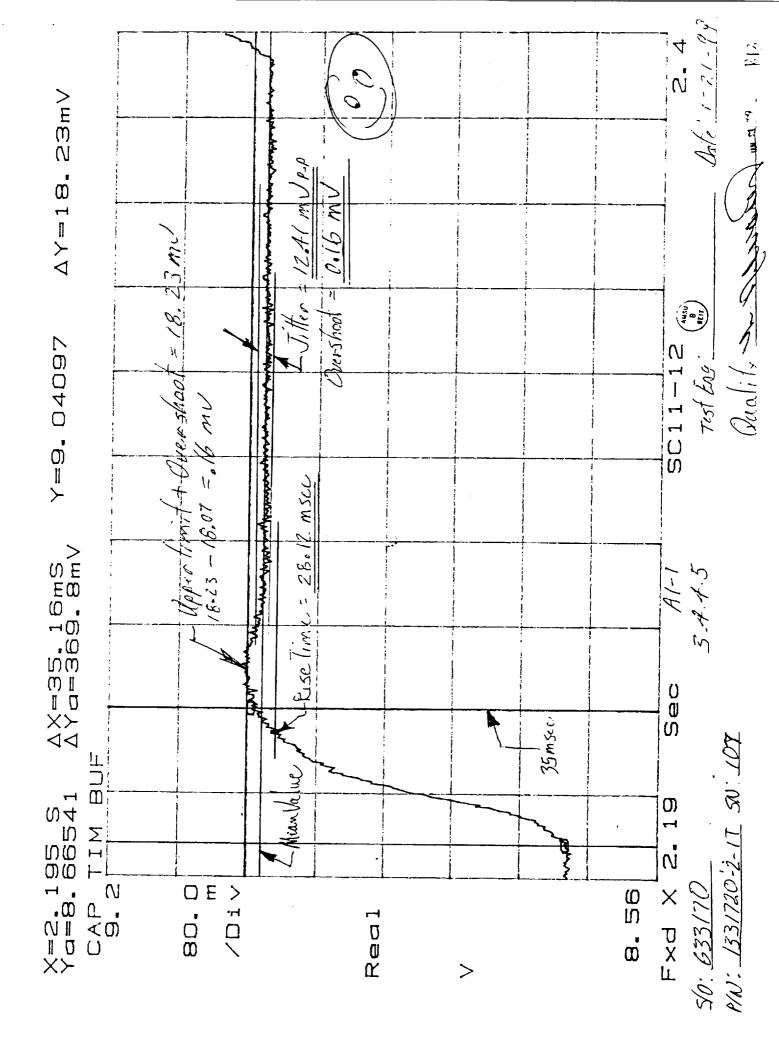


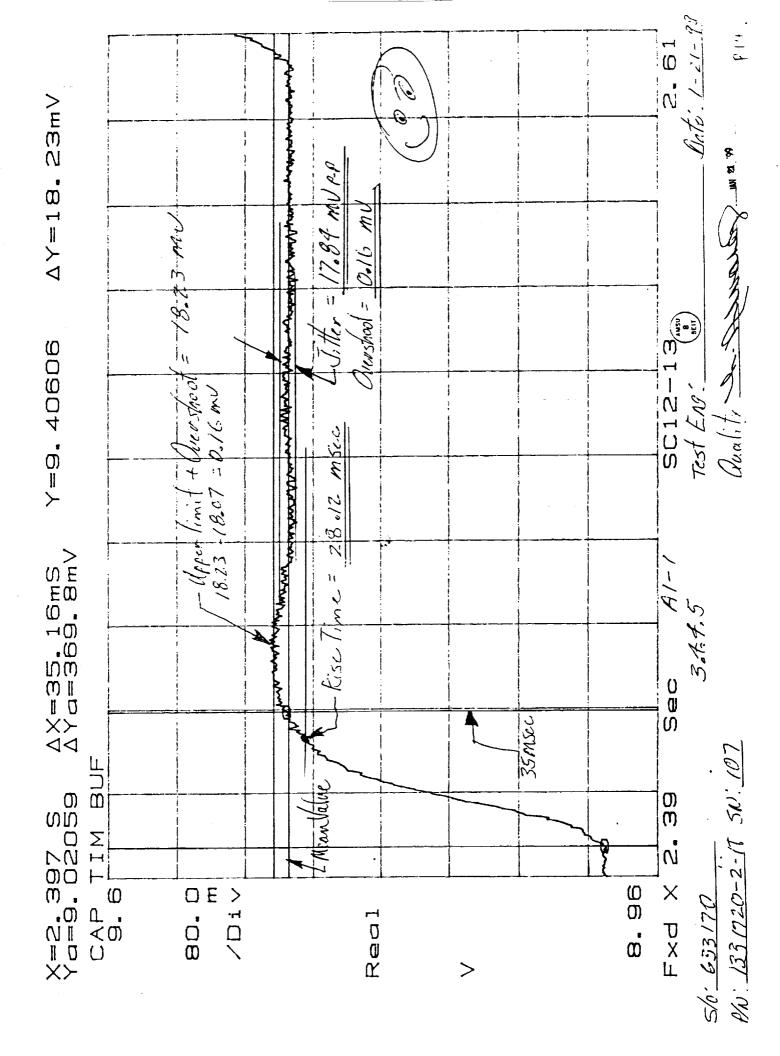


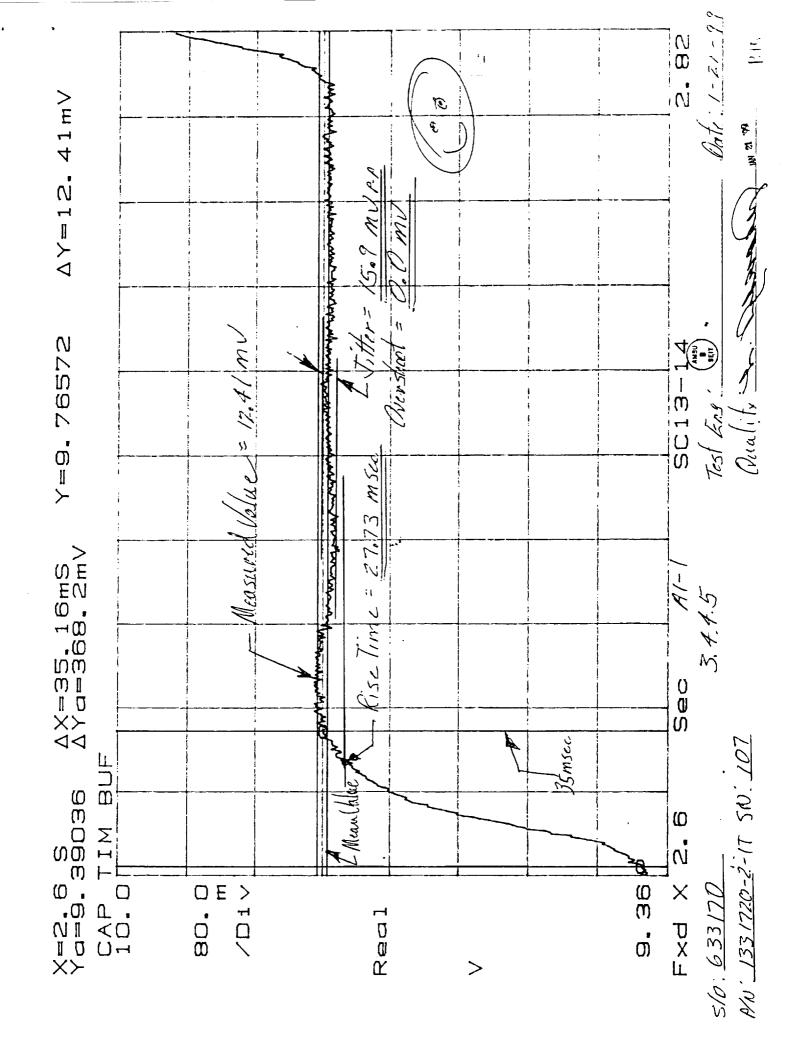


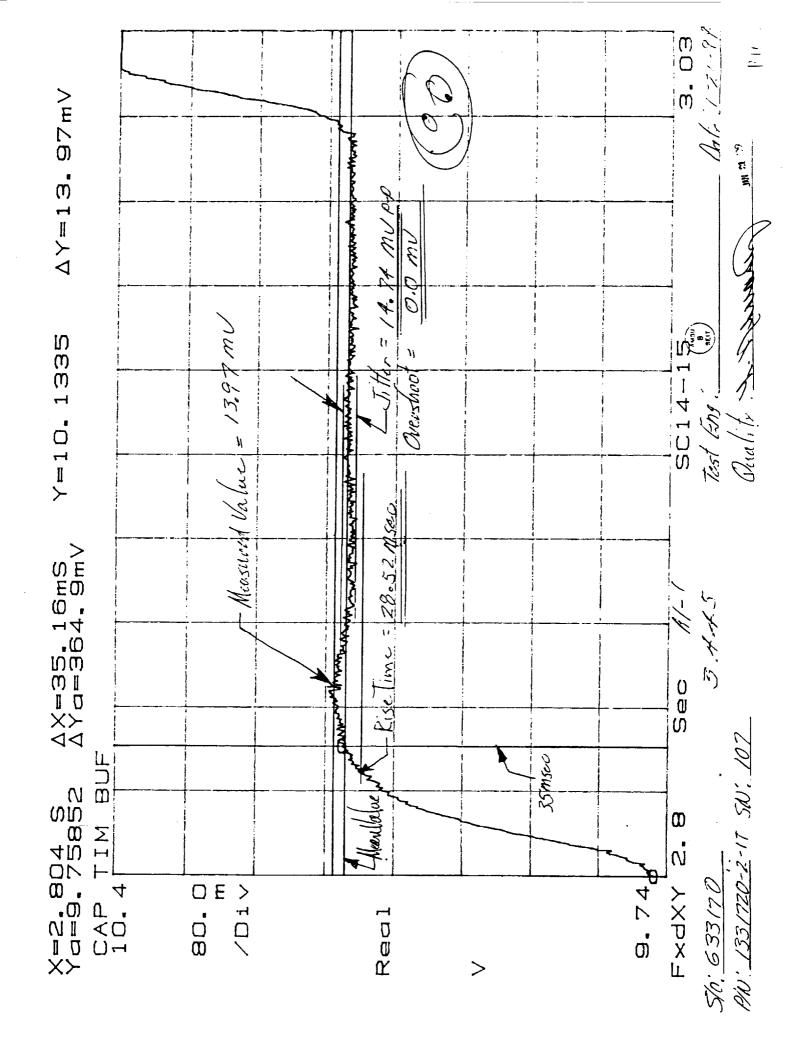


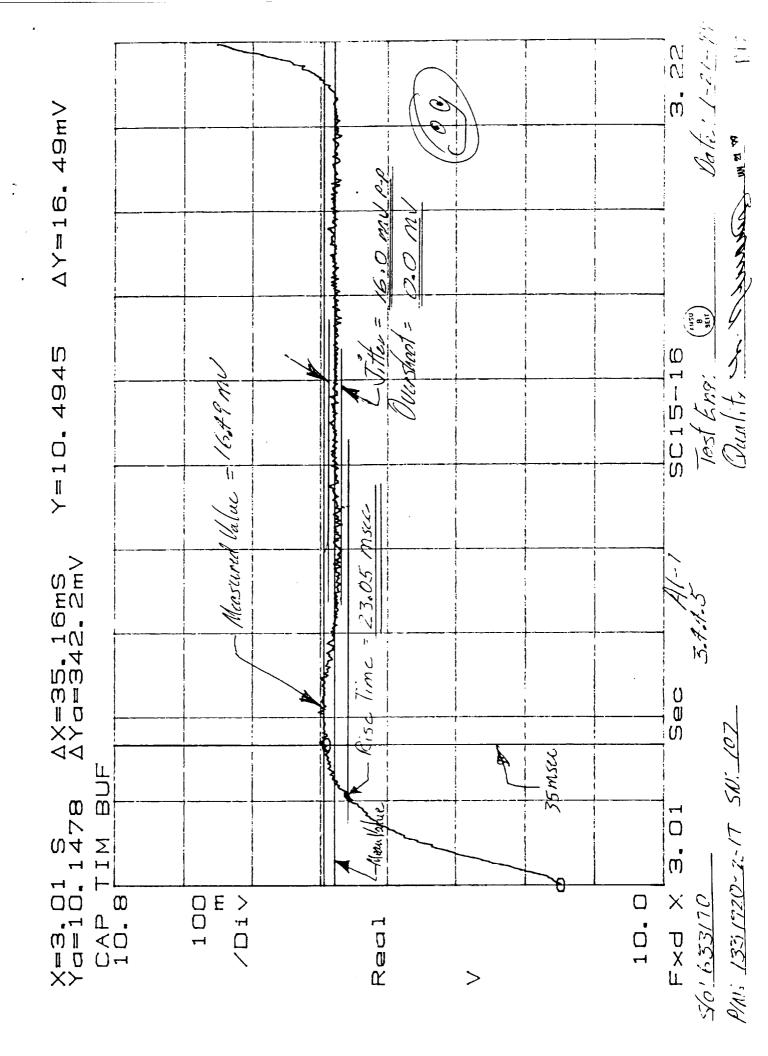


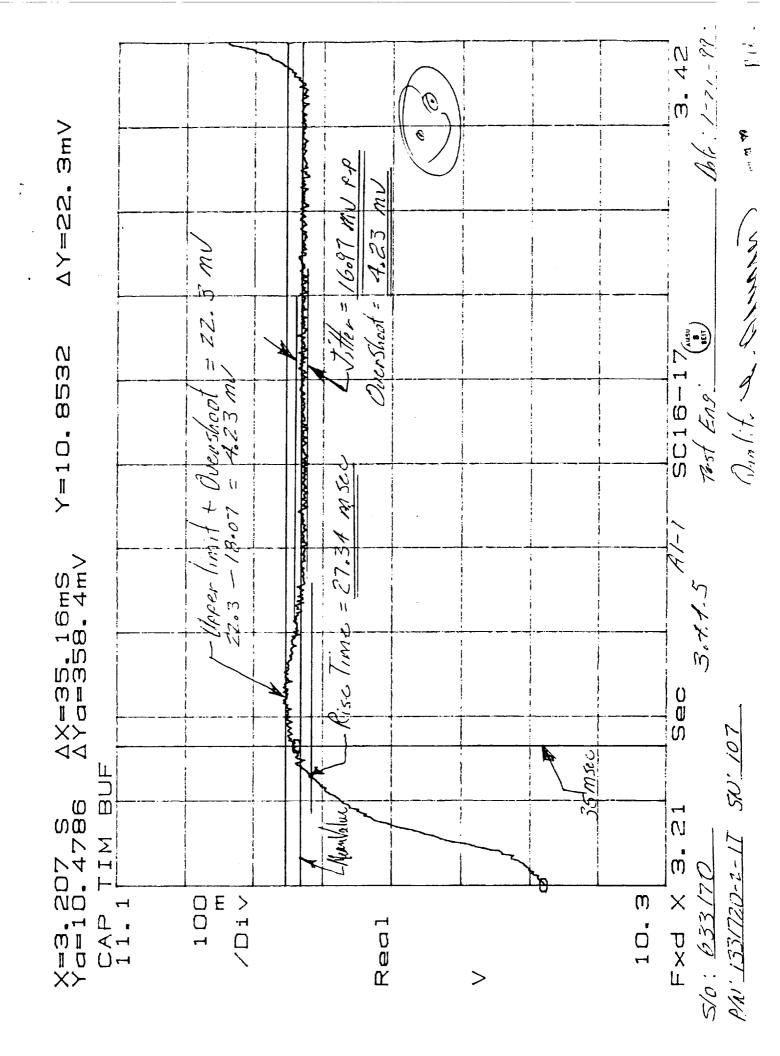


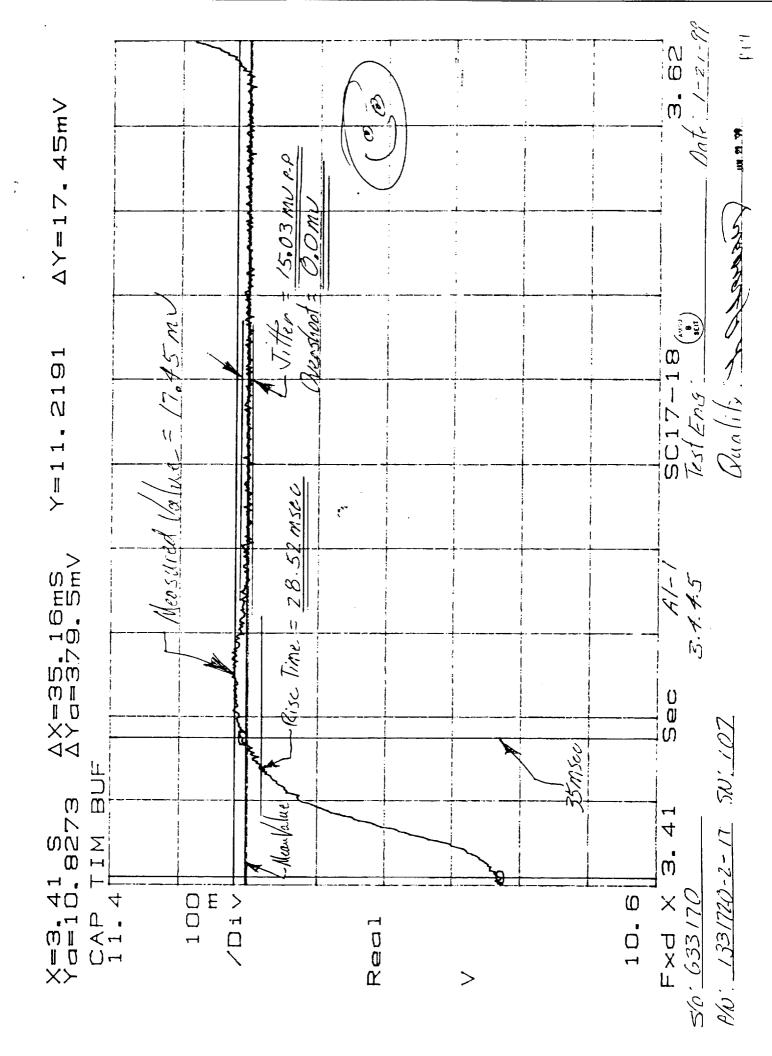


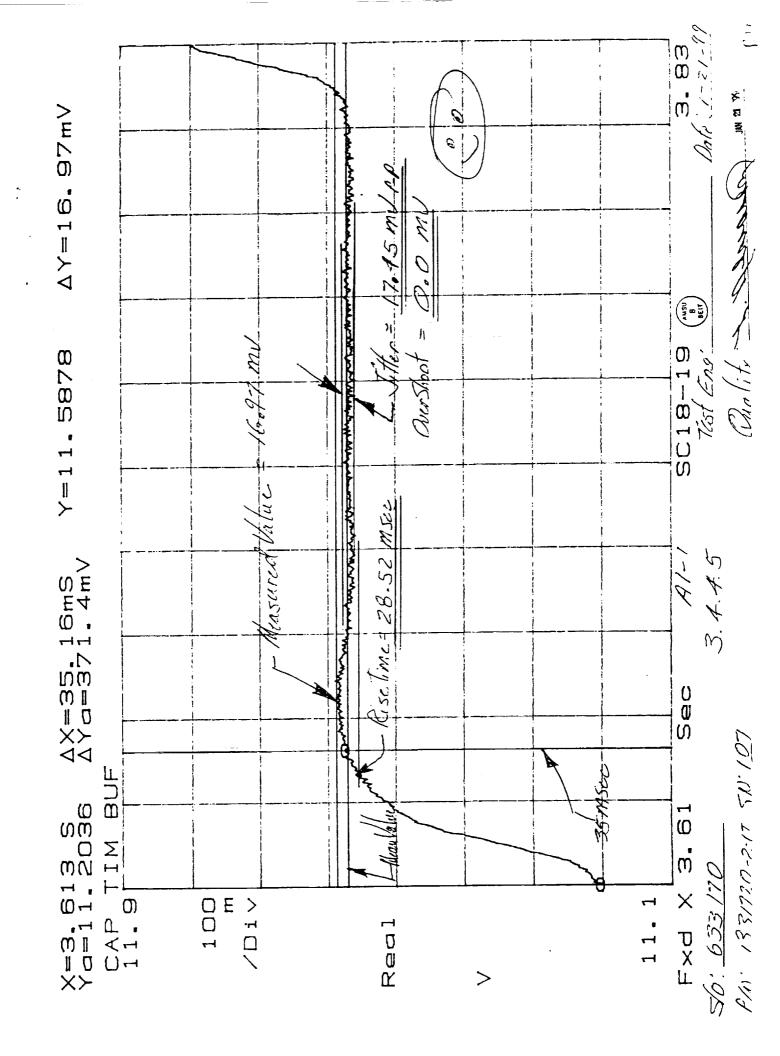


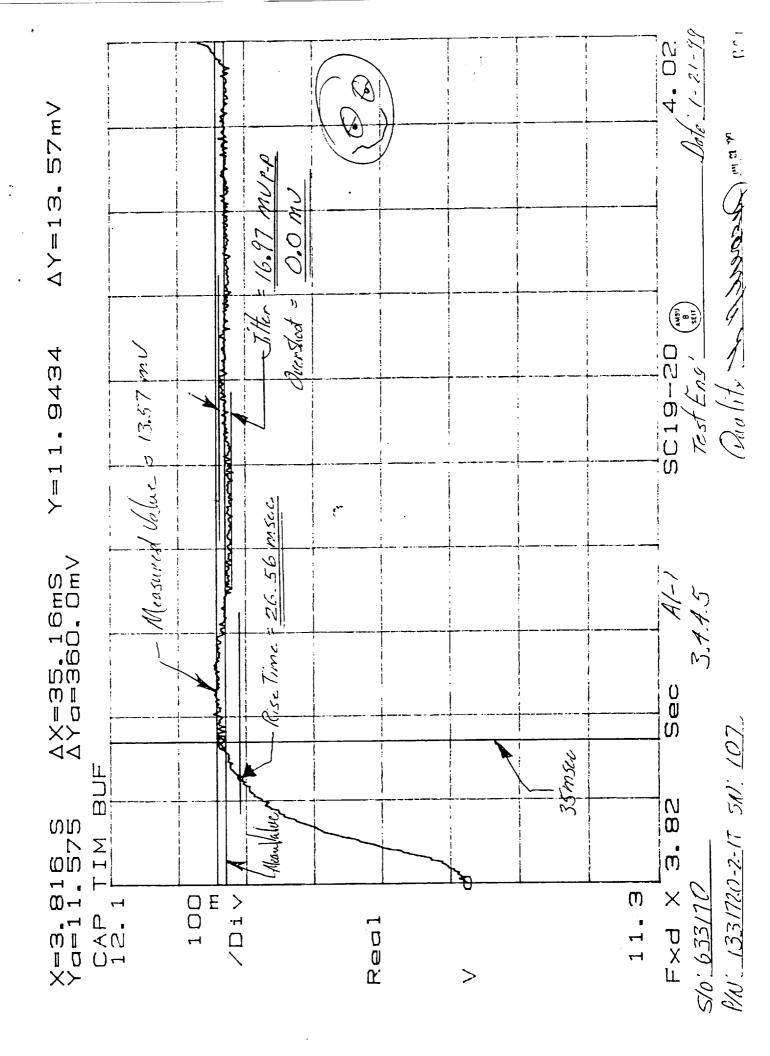


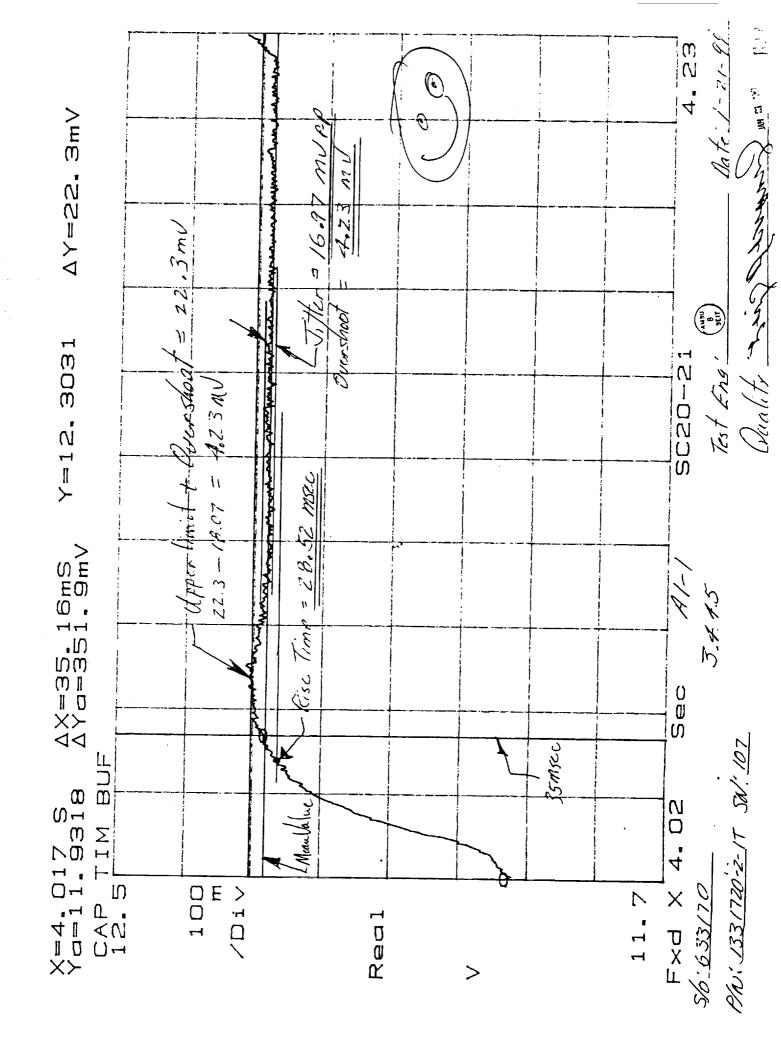


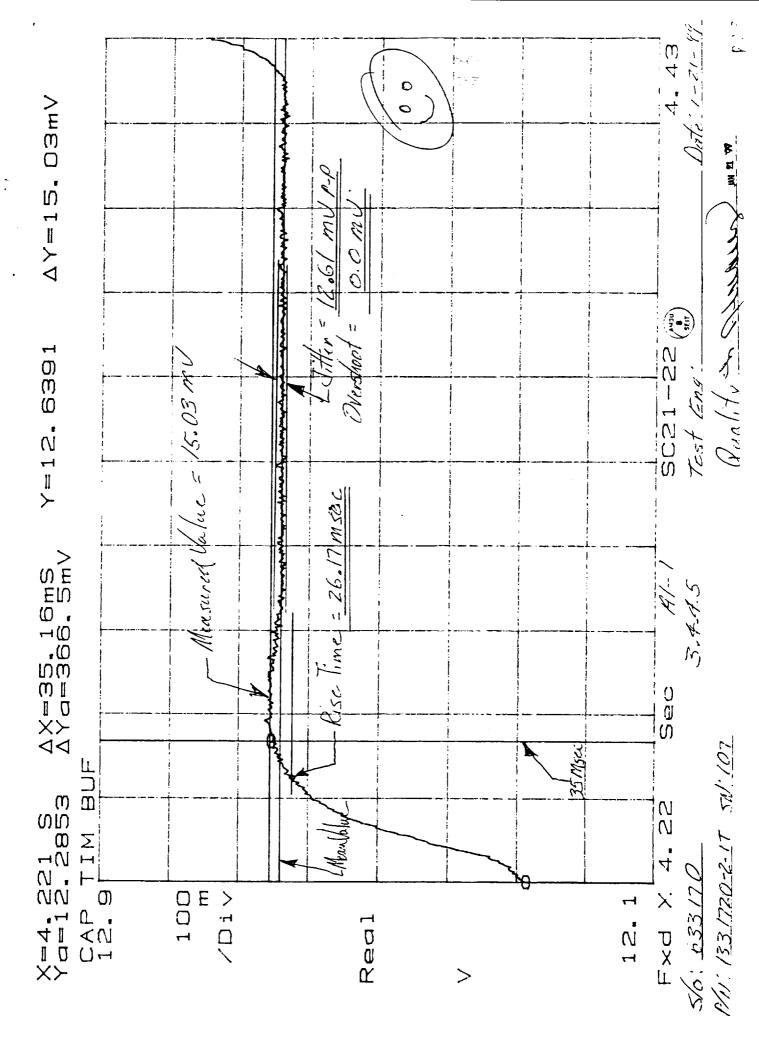


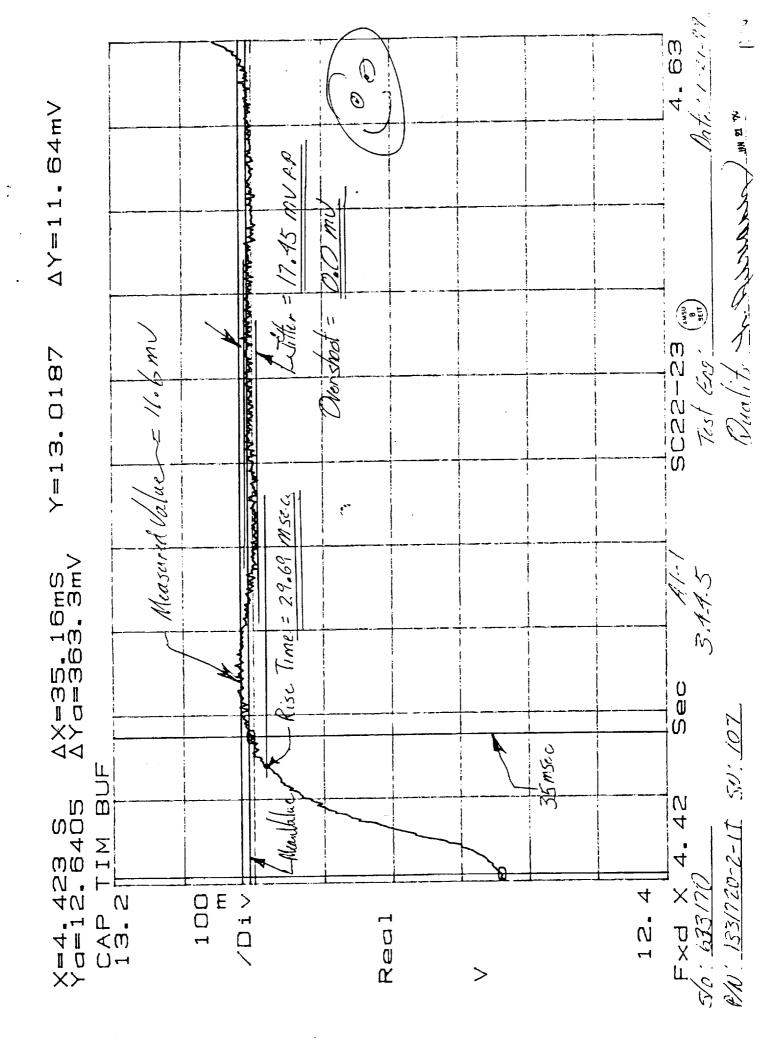


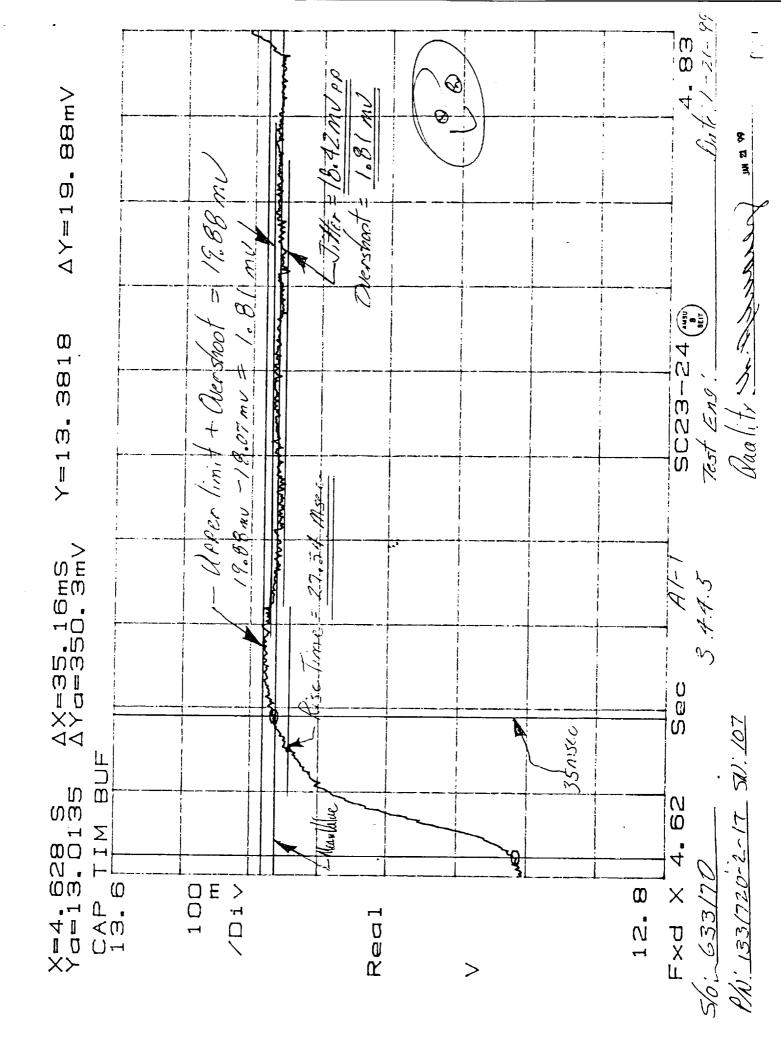


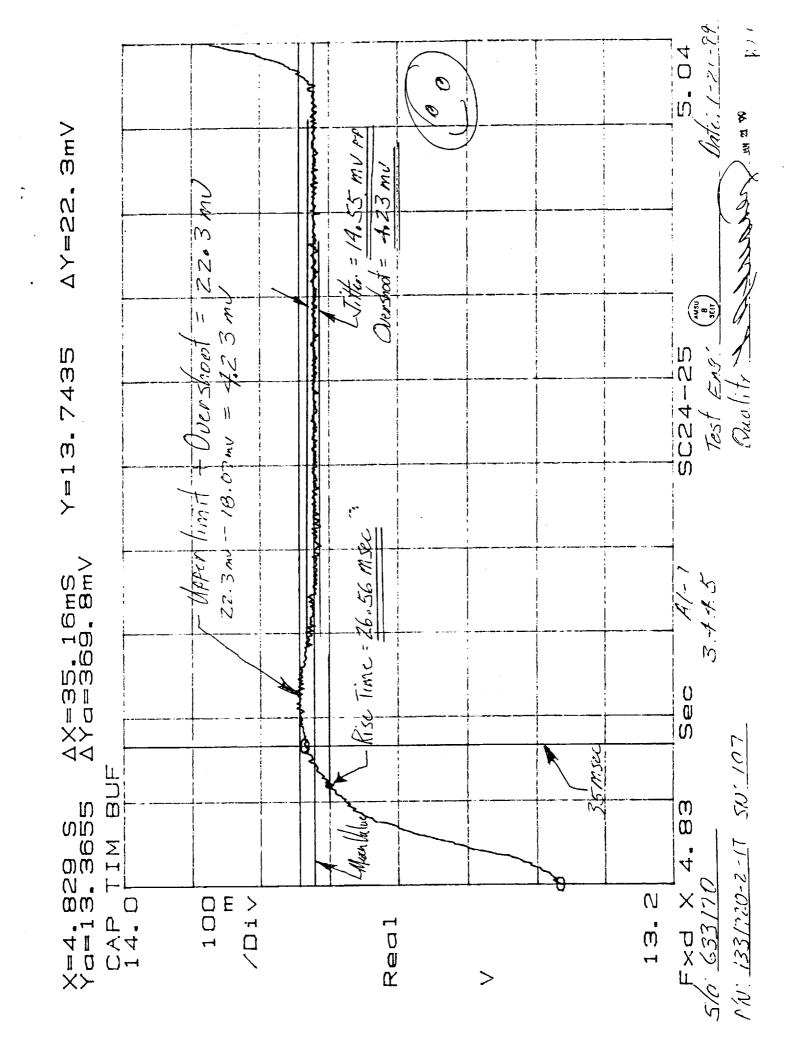


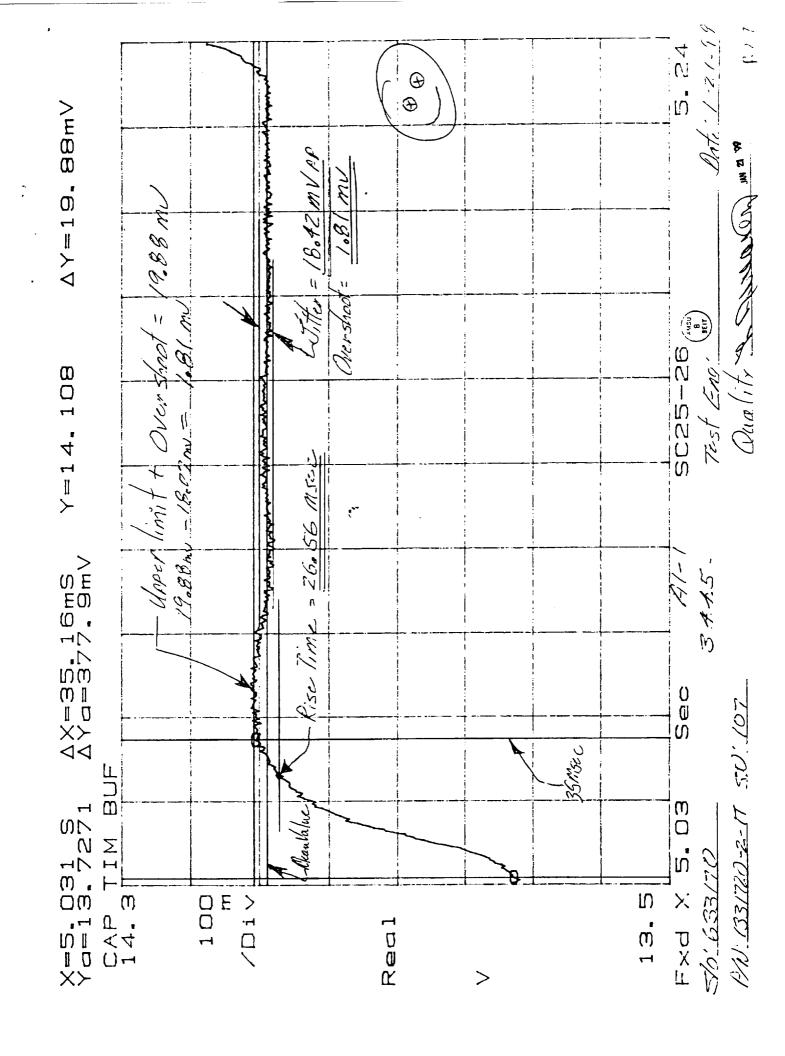


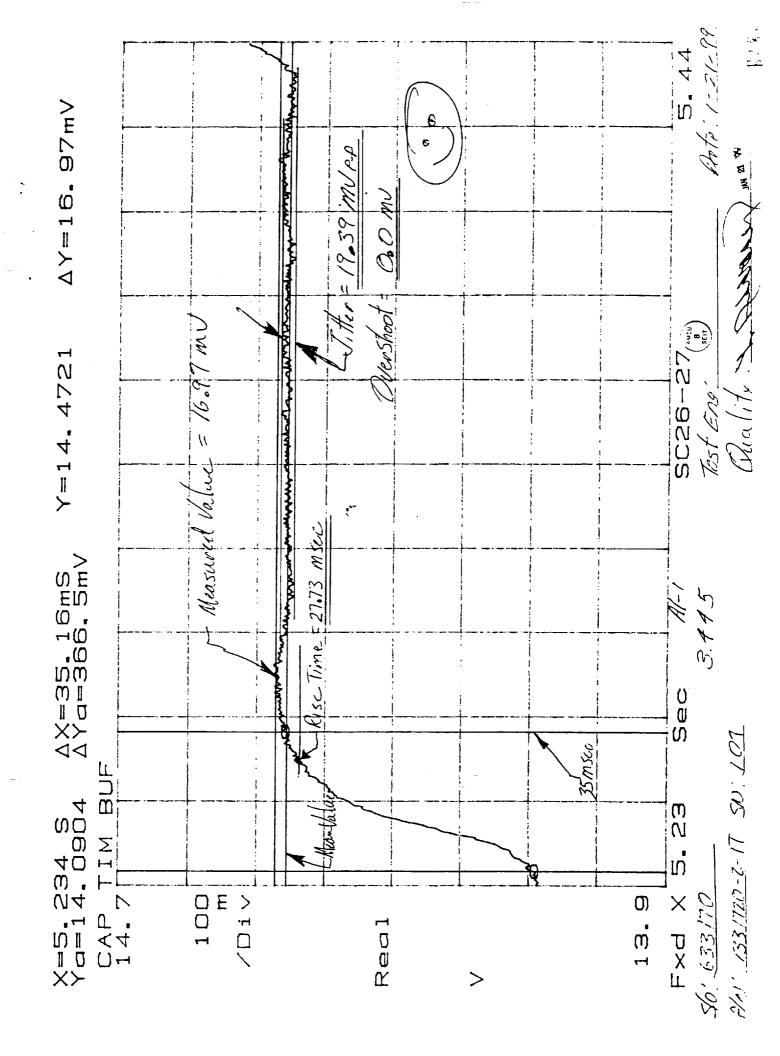


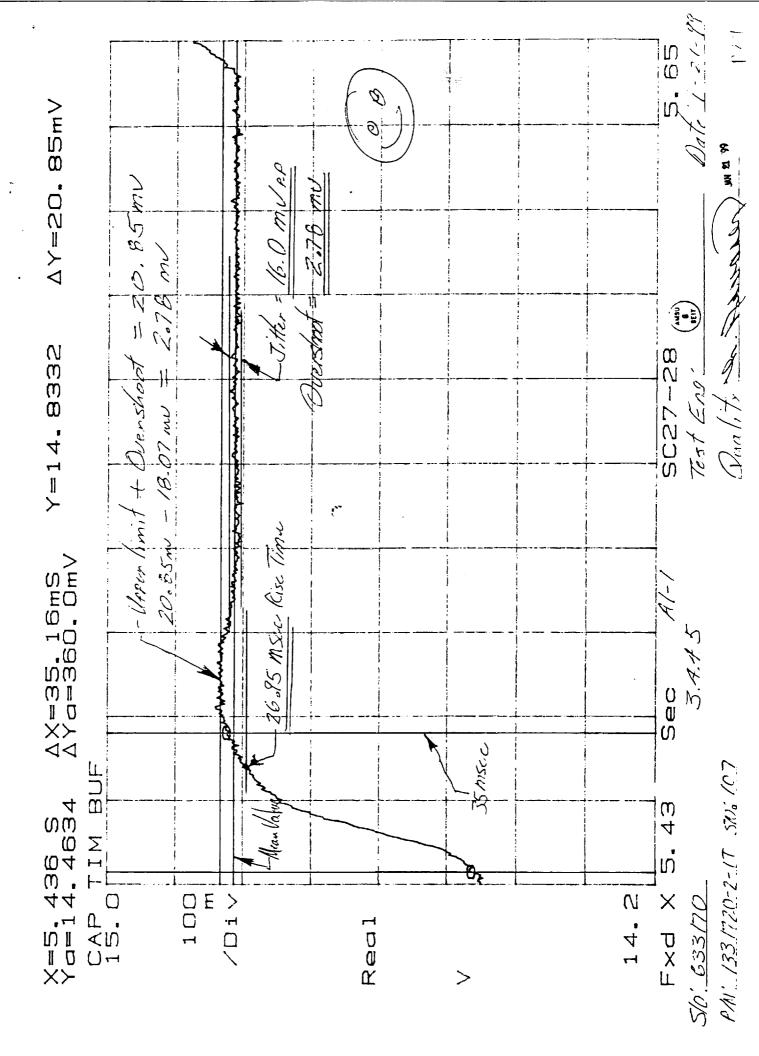


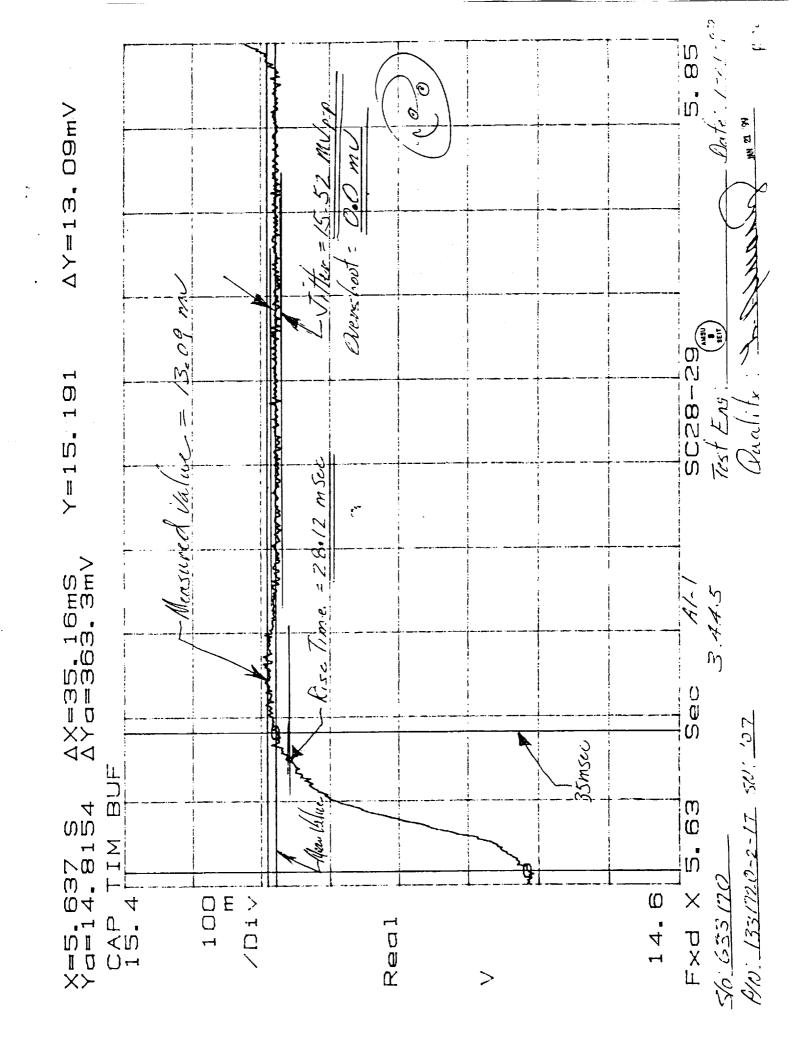


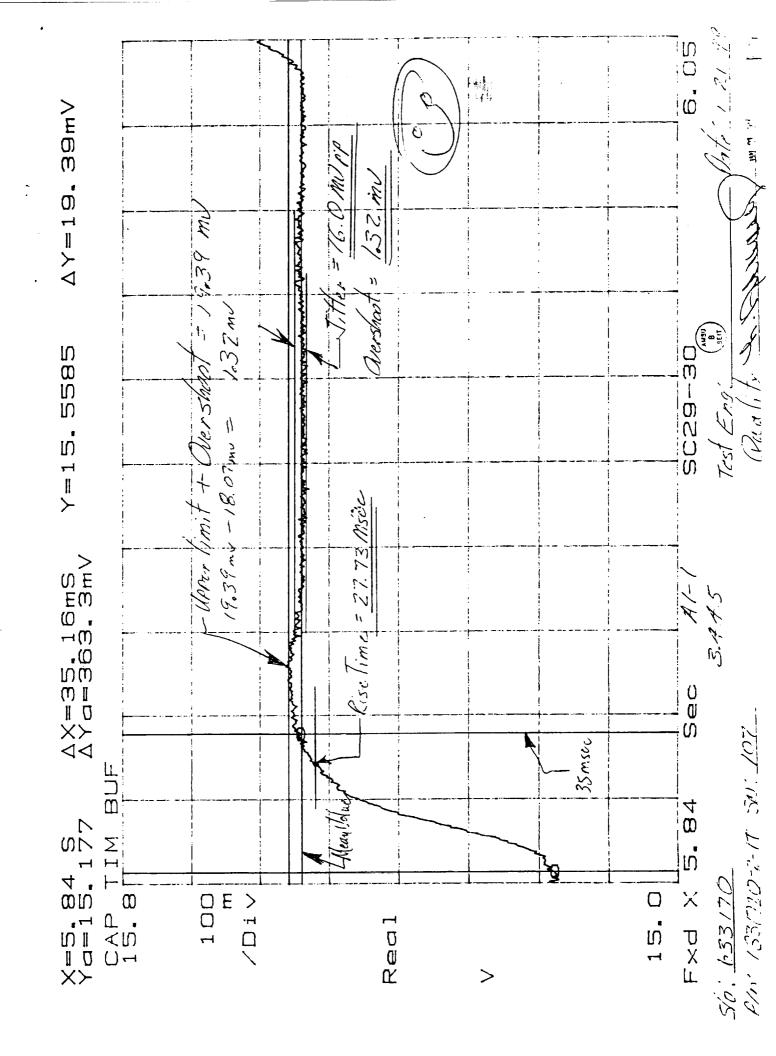


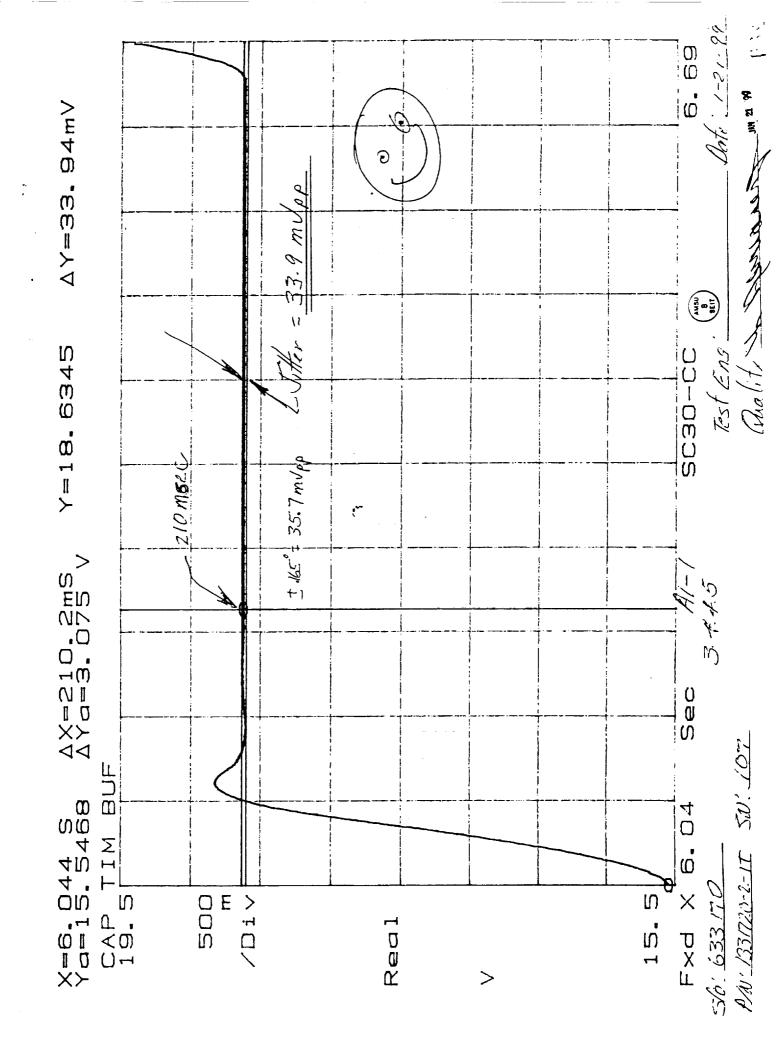


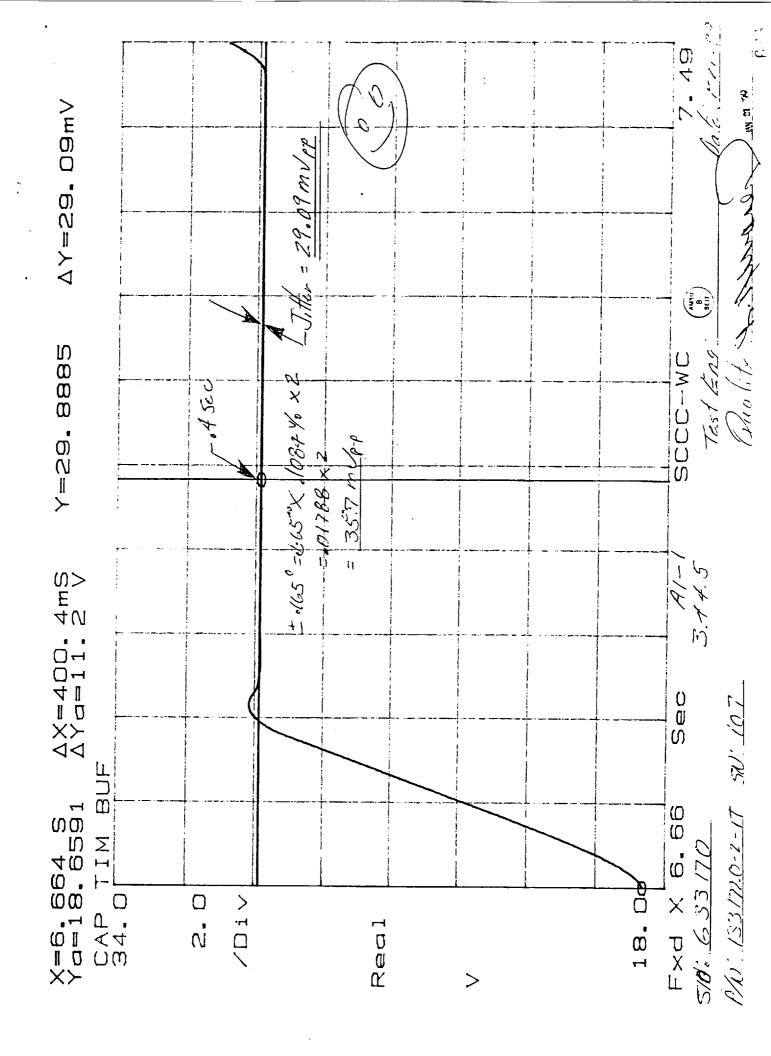




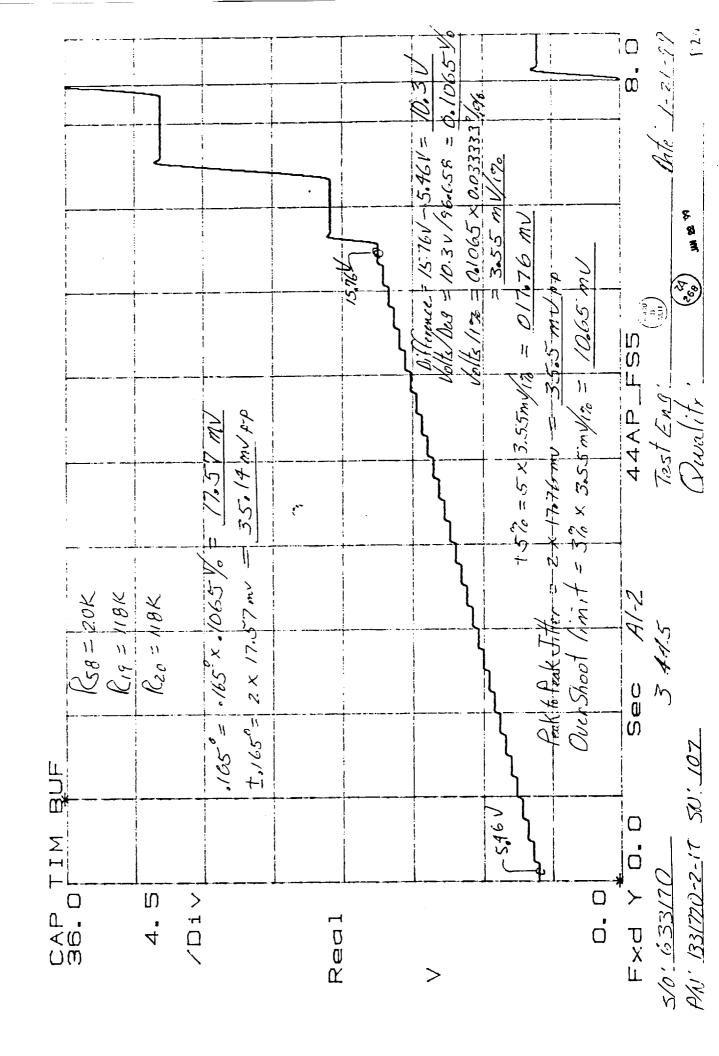




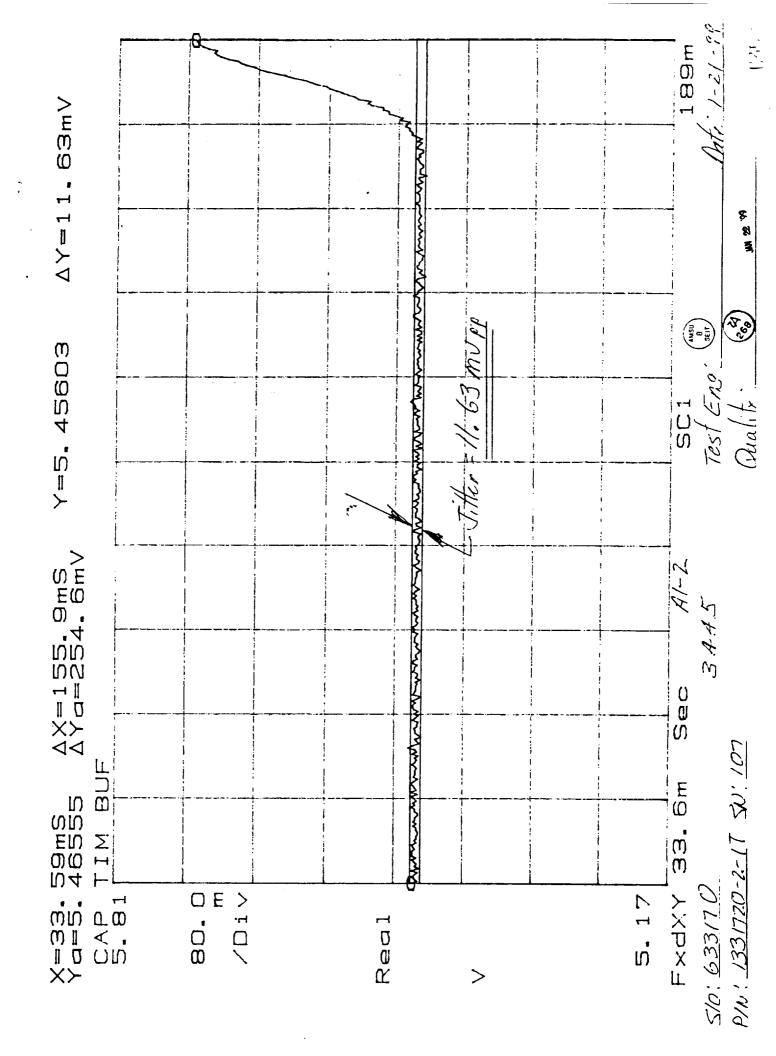


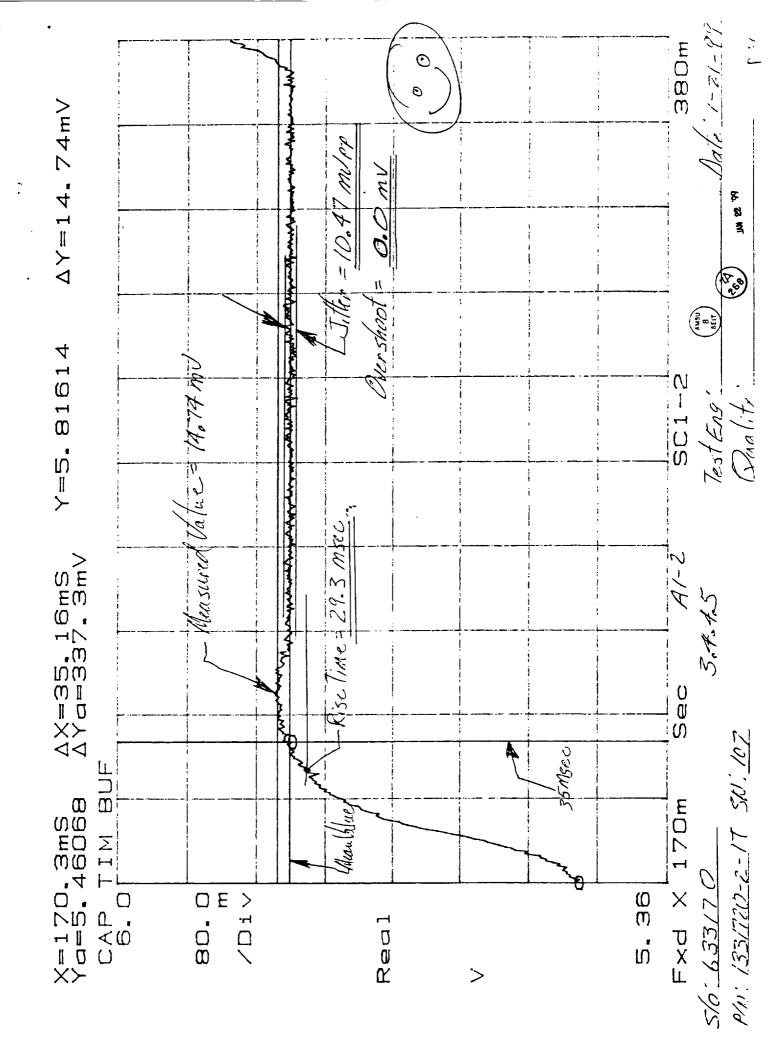


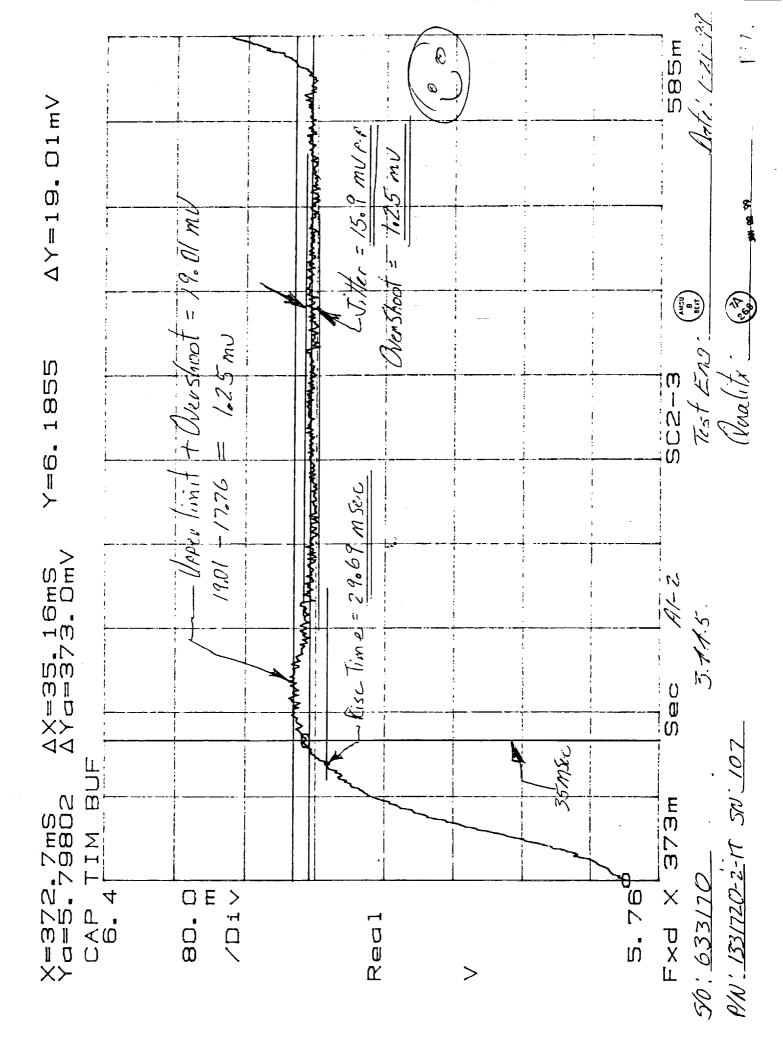
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т В В	CENTER 500 Hz	ţu	SPAN 1. OKHN	BW 1.87 Hz
	REC LGTH 800mS	Δt 391μS		
TRIGGER	TYPE External	LEVEL O.O VPK	SLOPE	
INPUT CH T	RANGE 31.7 VPK AutoRng^	ENG UNITS 1.0 V/EU 1.0 V/EU	COUPLING DC (Gnd) DC (Gnd)	DELAY 0.0 S 0.0 S
SOURCE.	TYPE Off		LEVEL O.O VPK	OFFSET O.O <pk< td=""></pk<>
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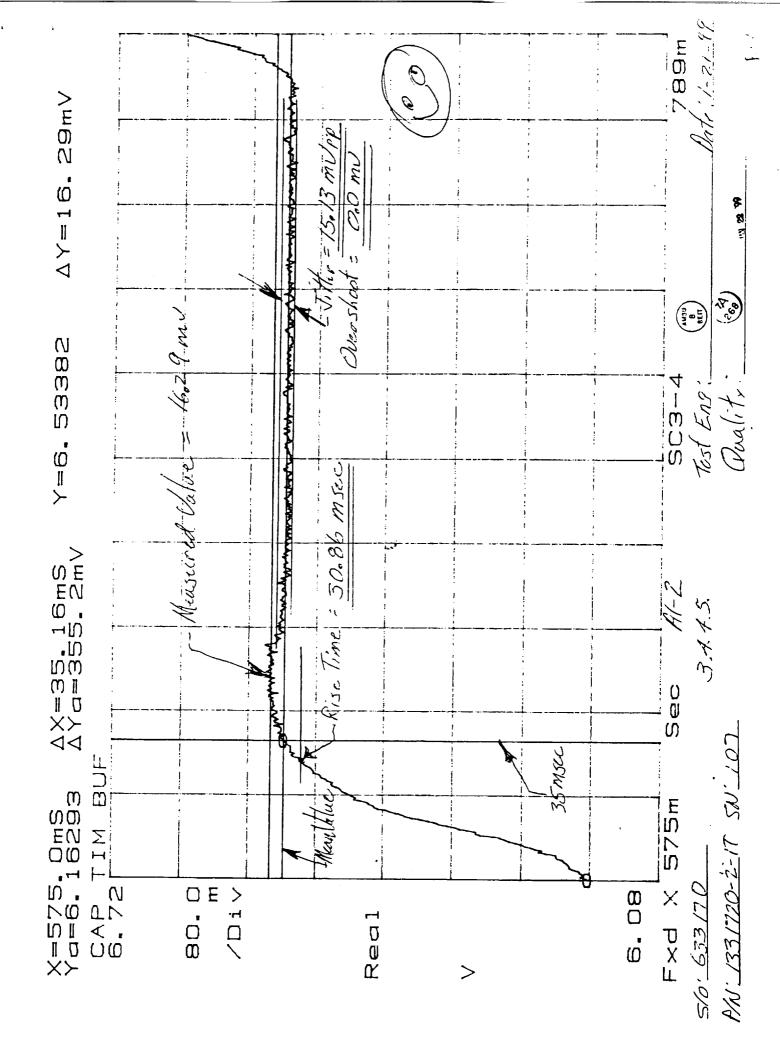


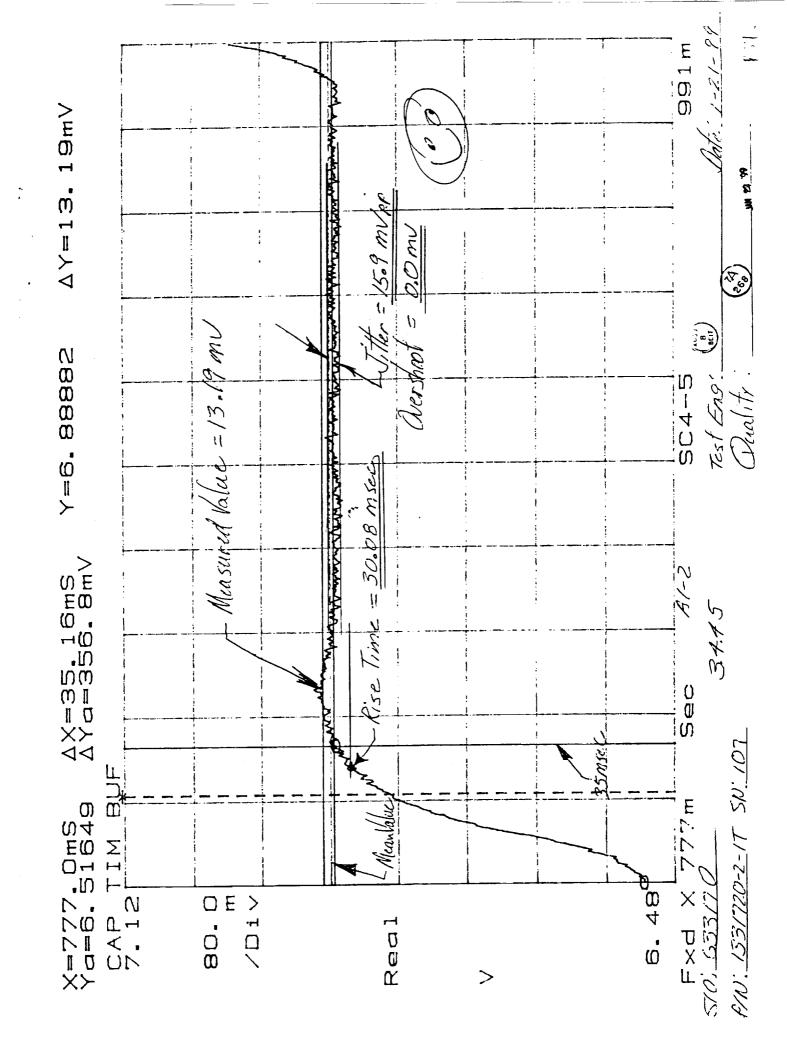
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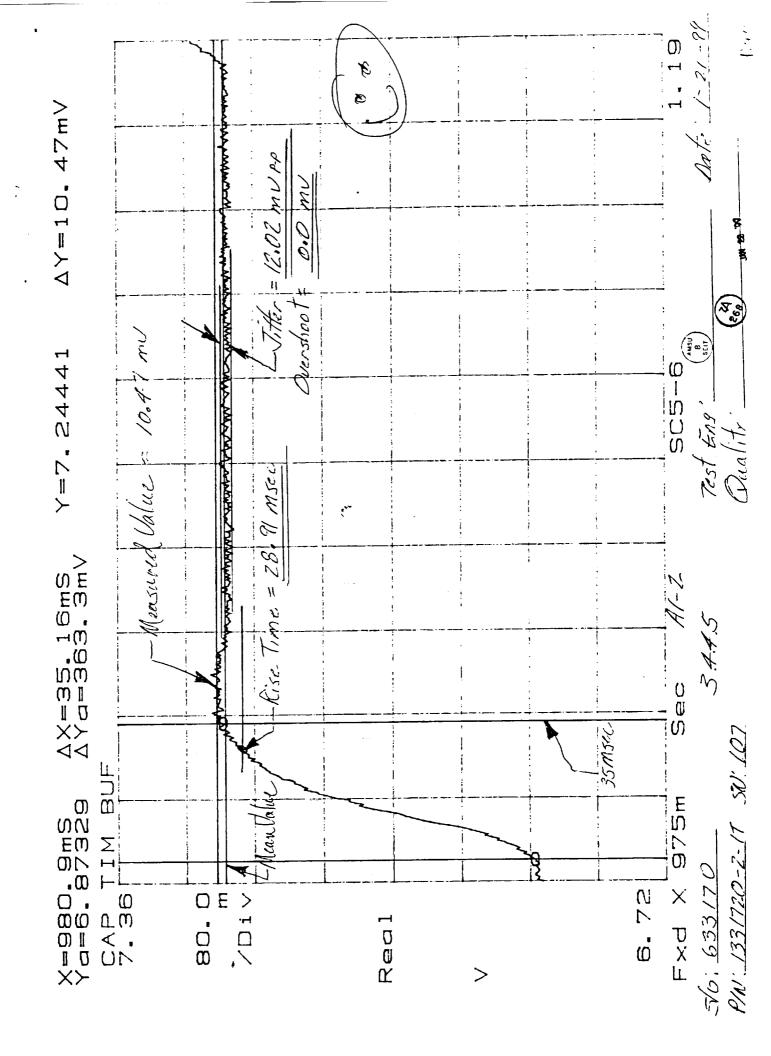


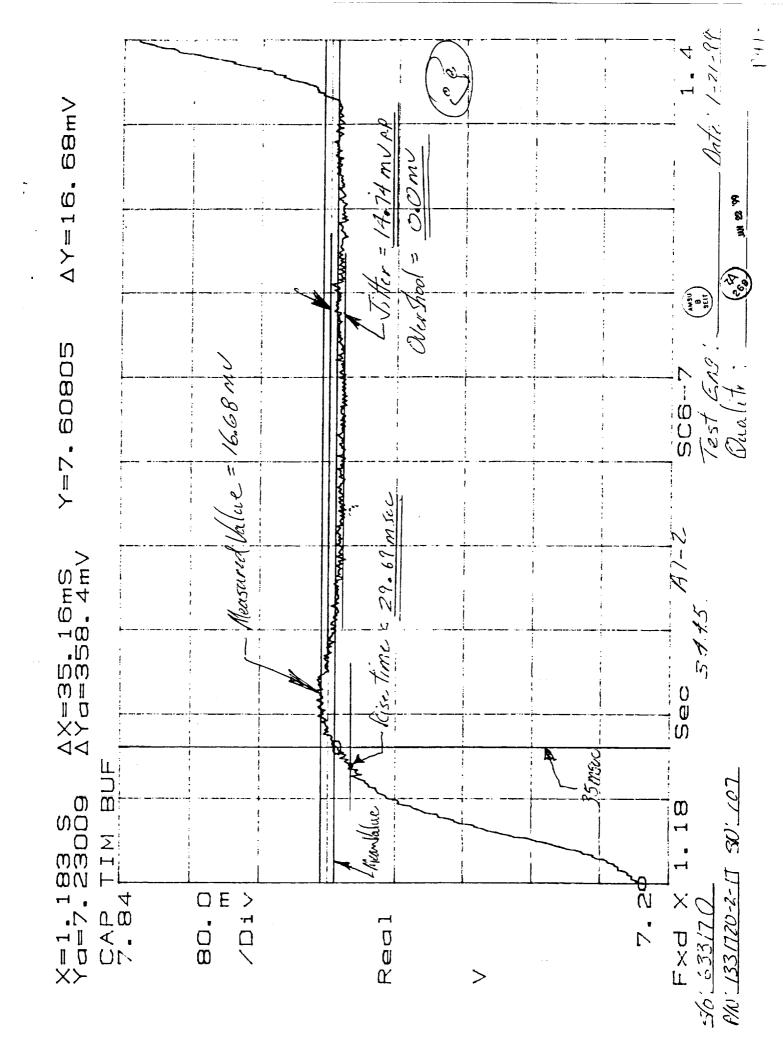


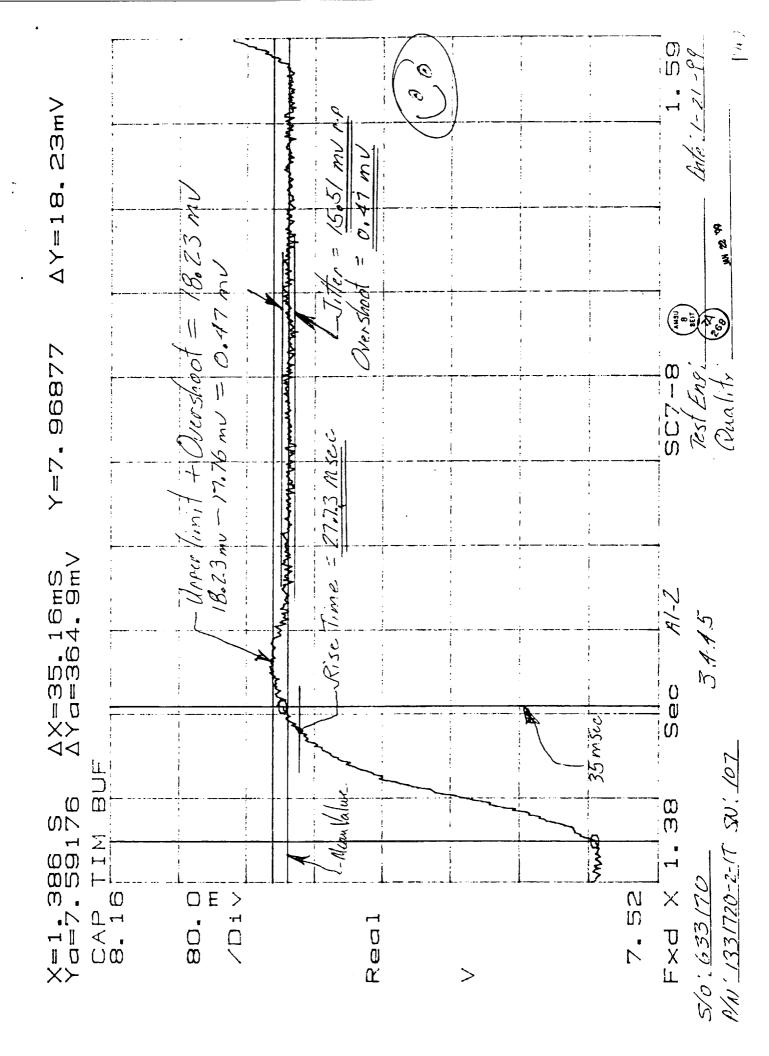


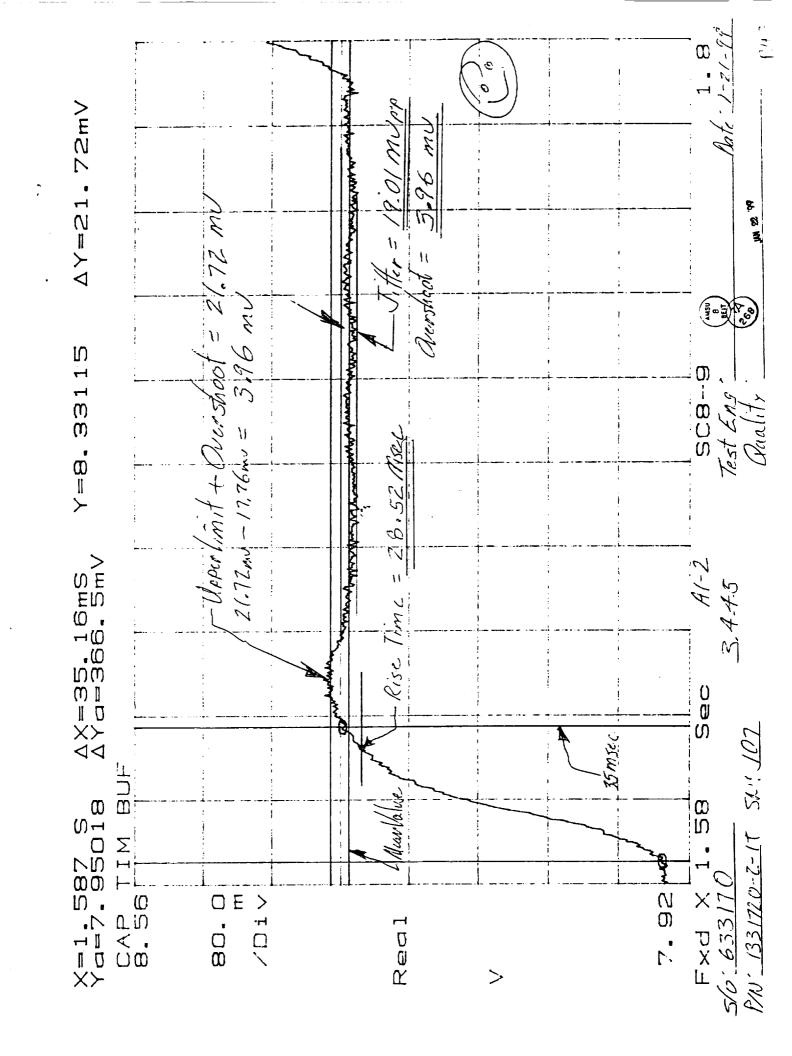


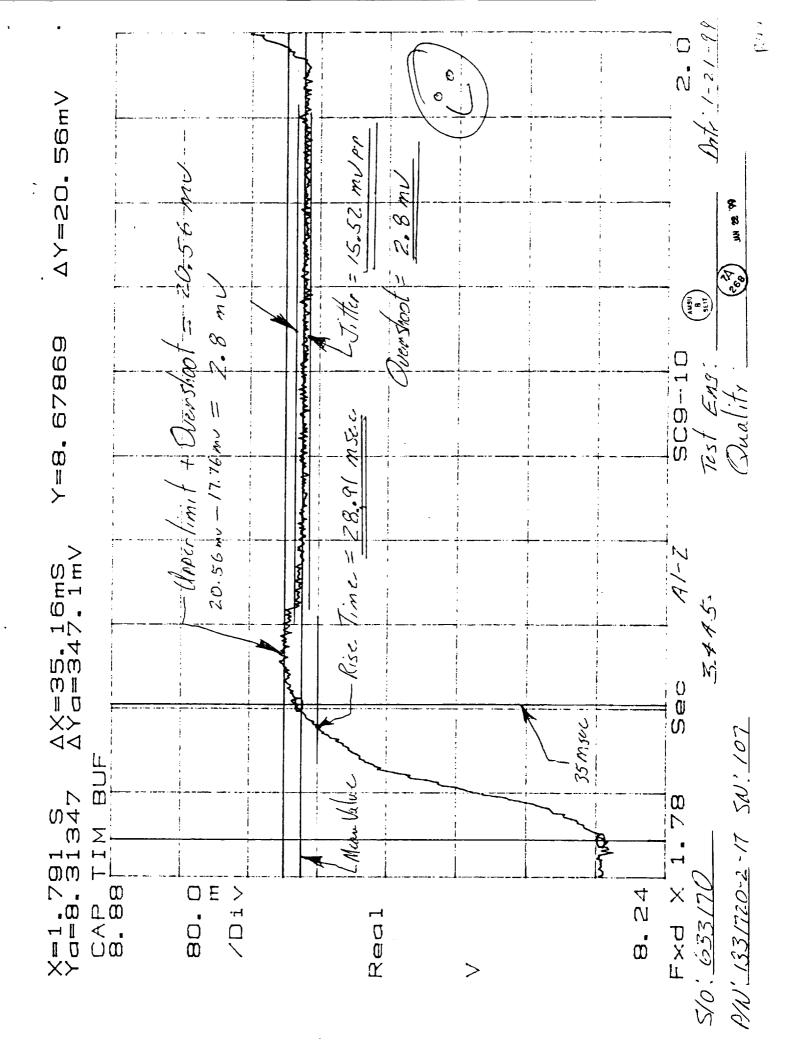


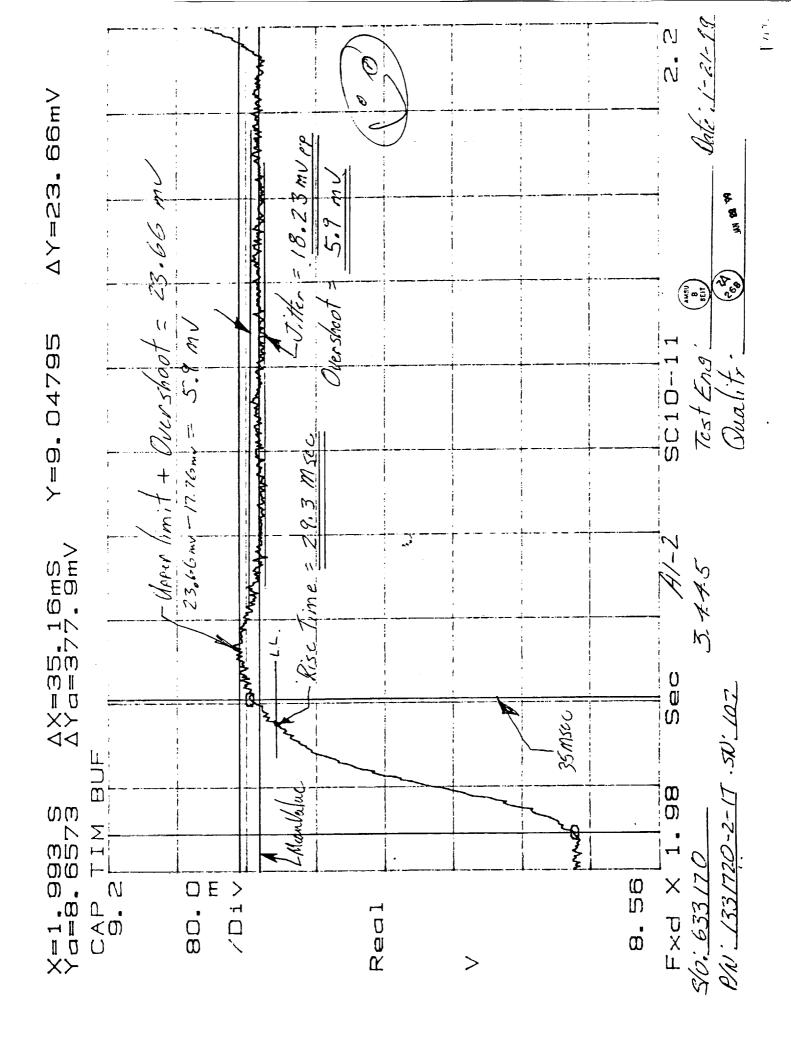


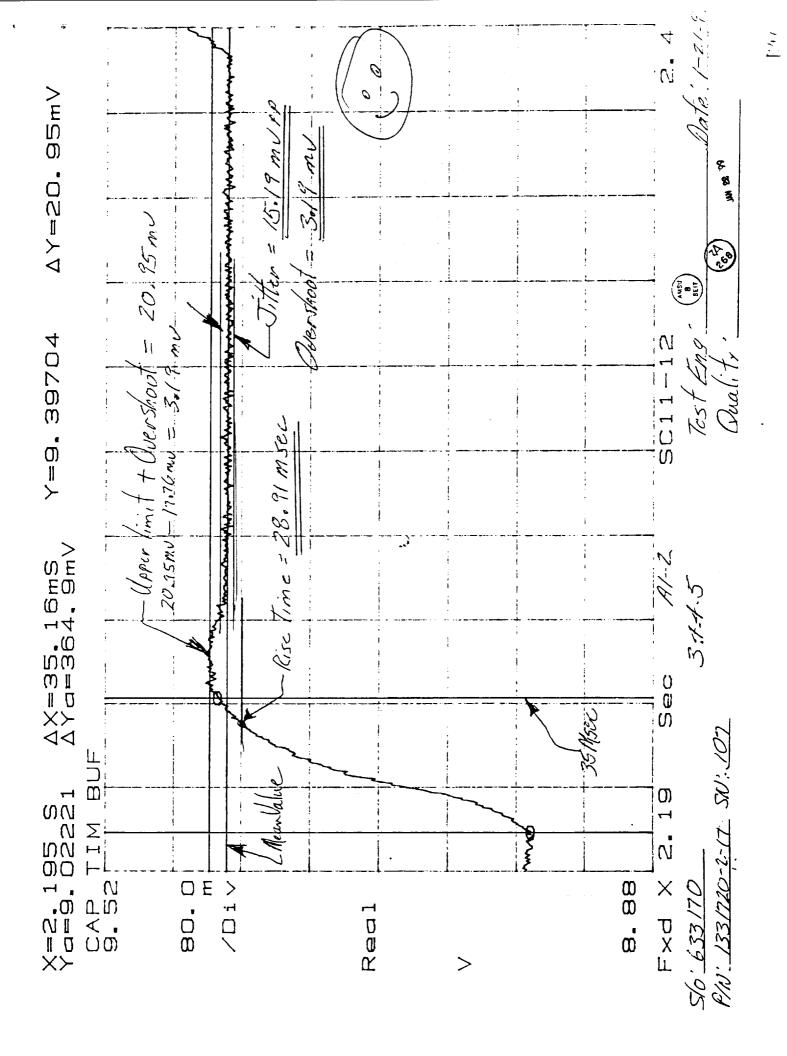


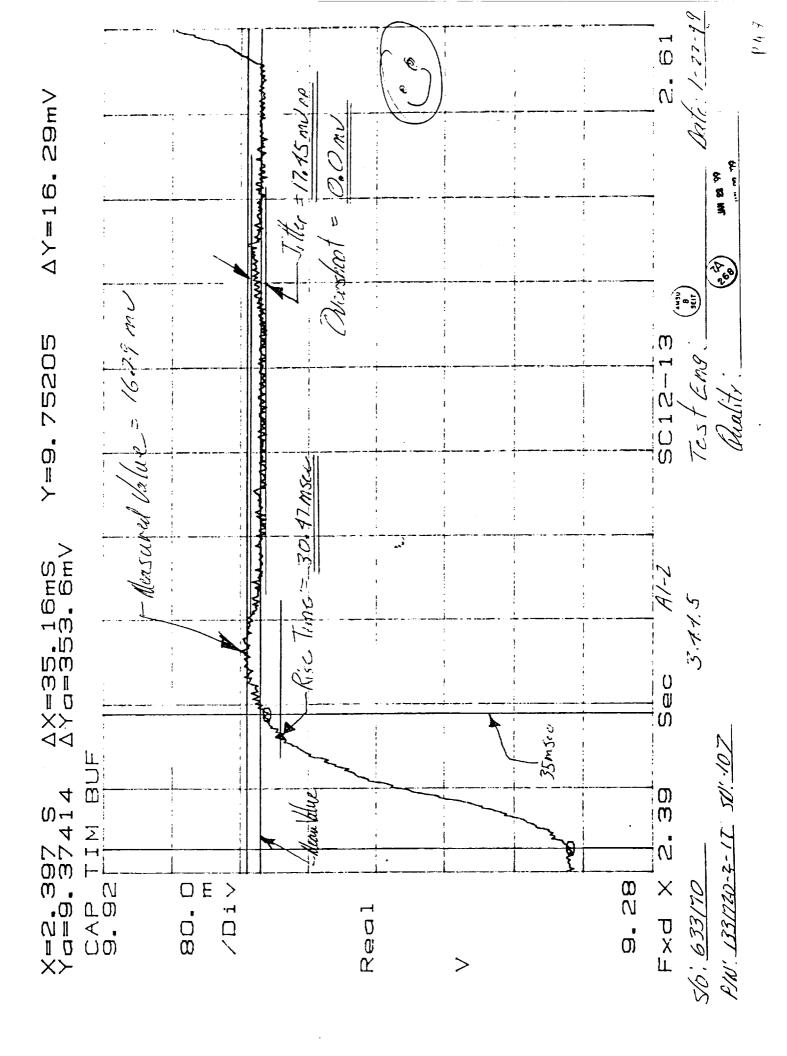


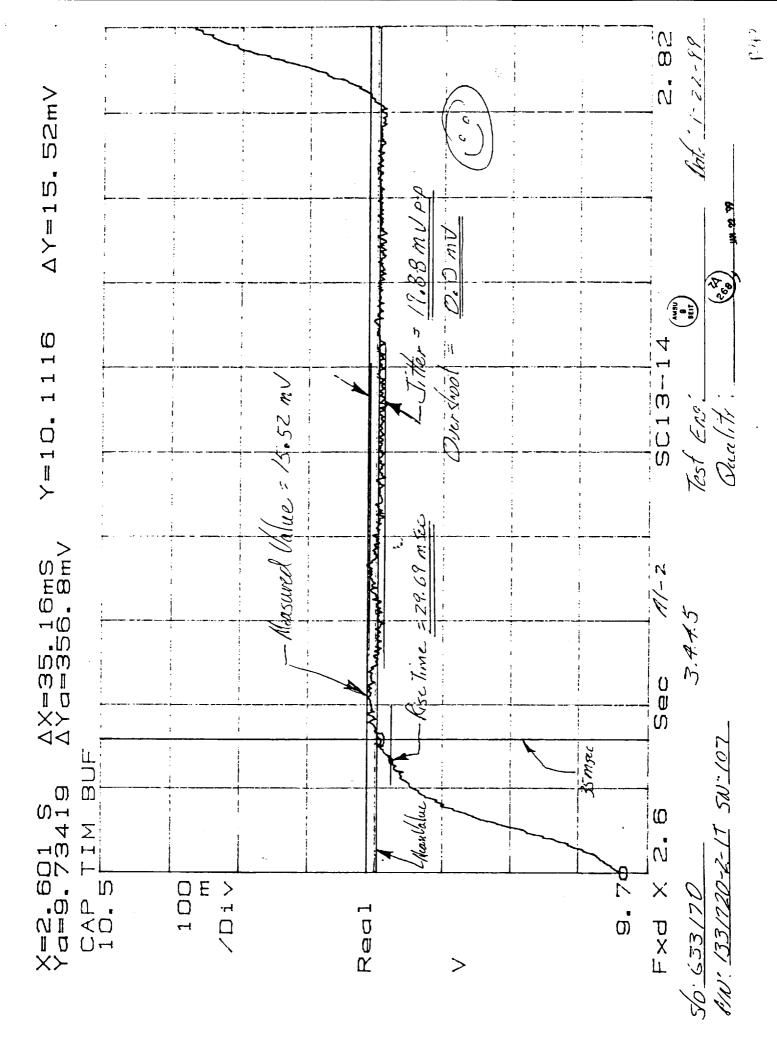


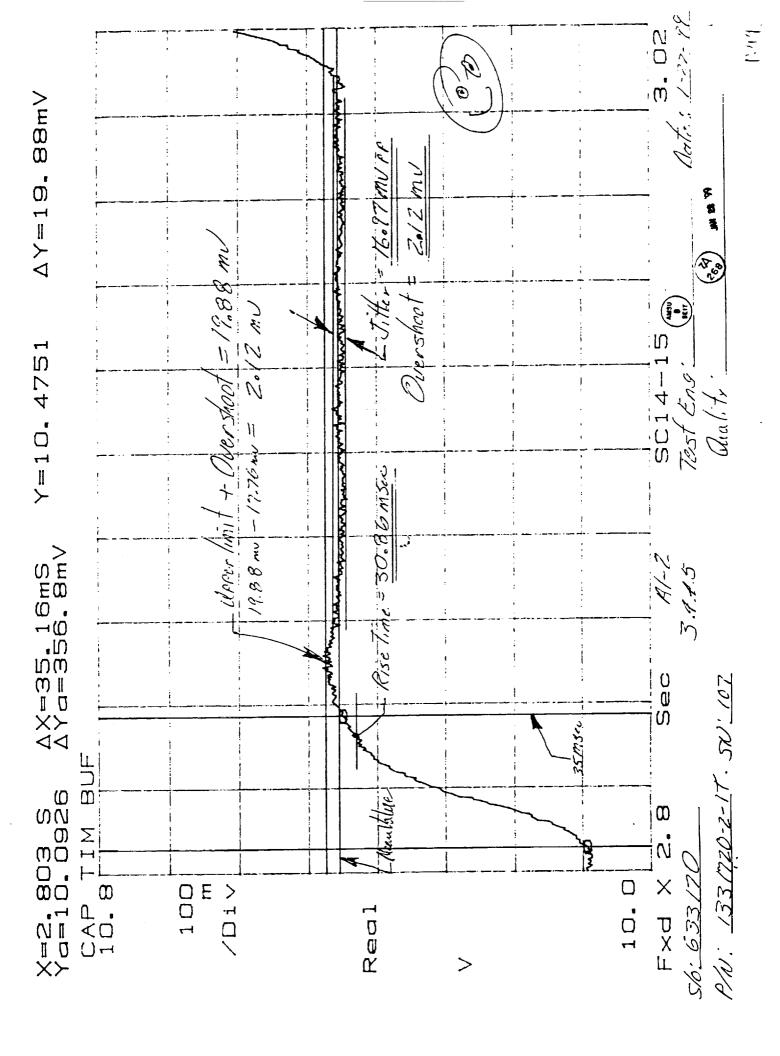


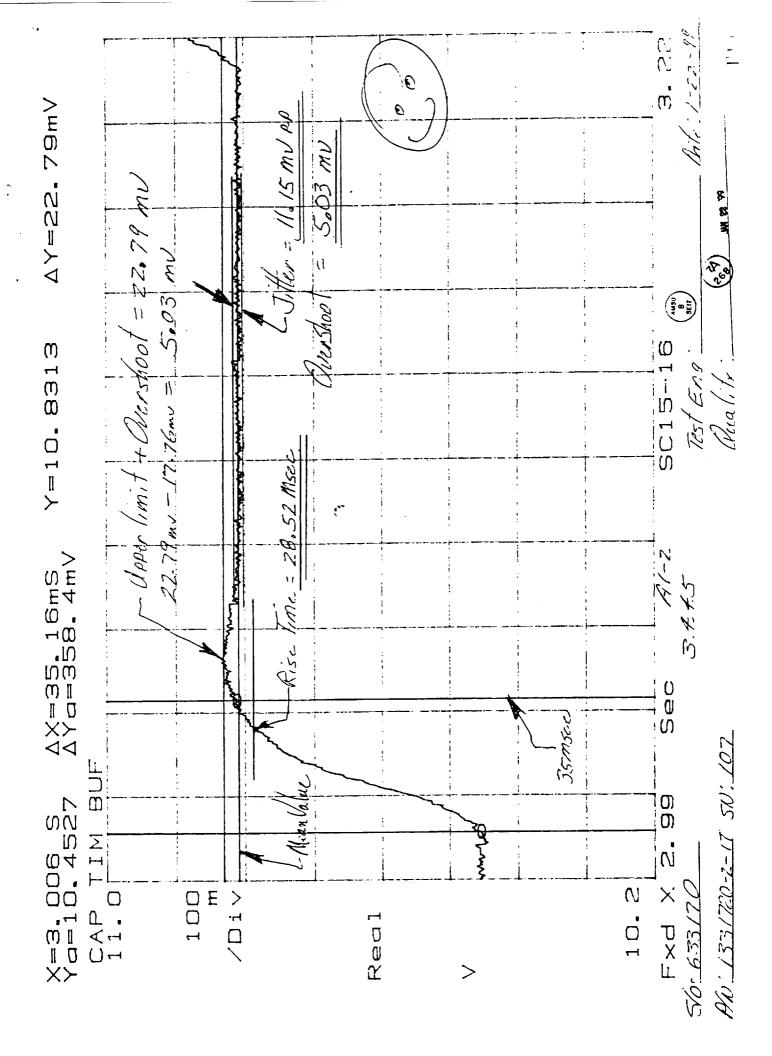


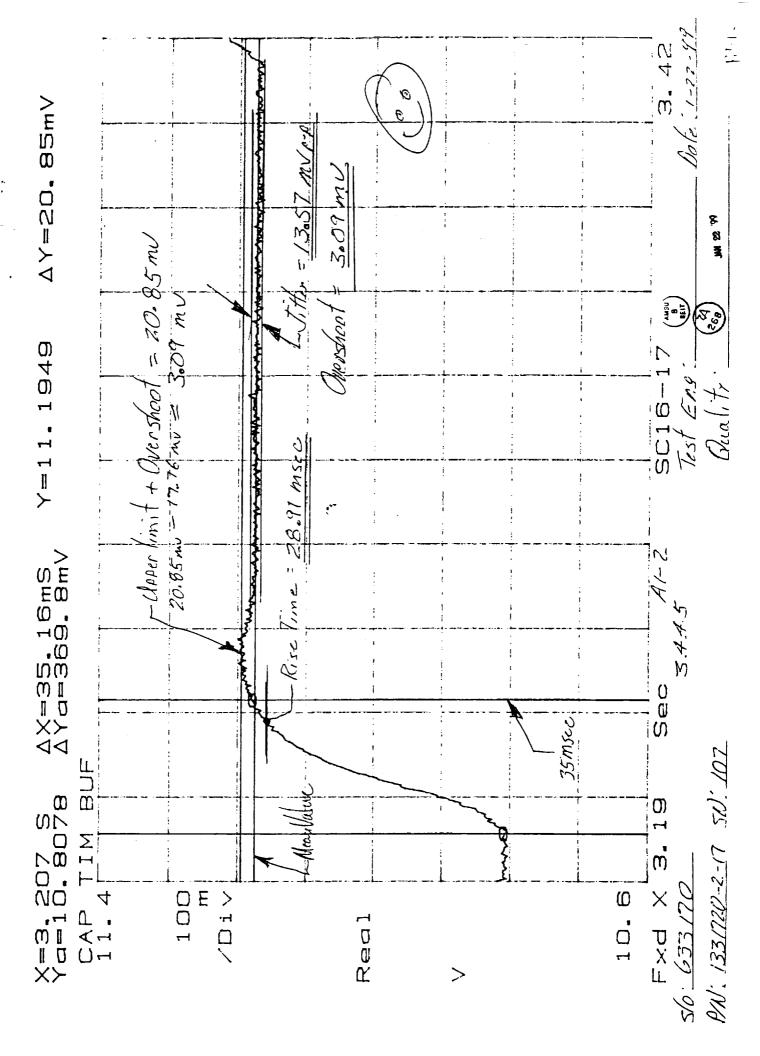


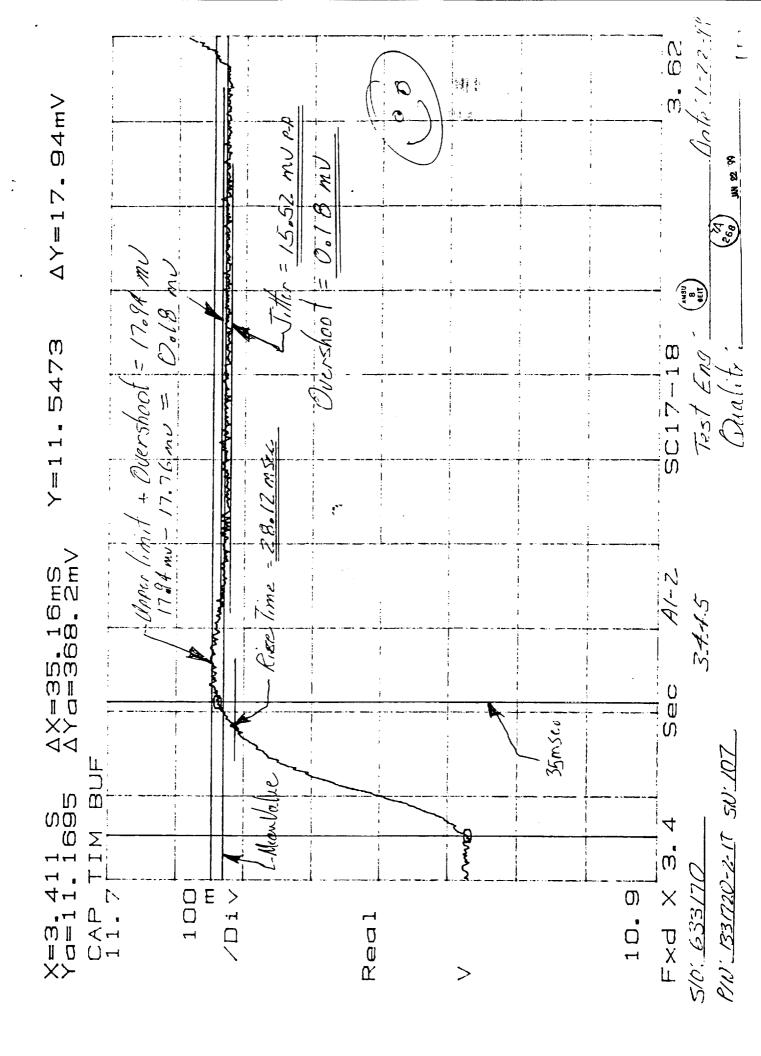


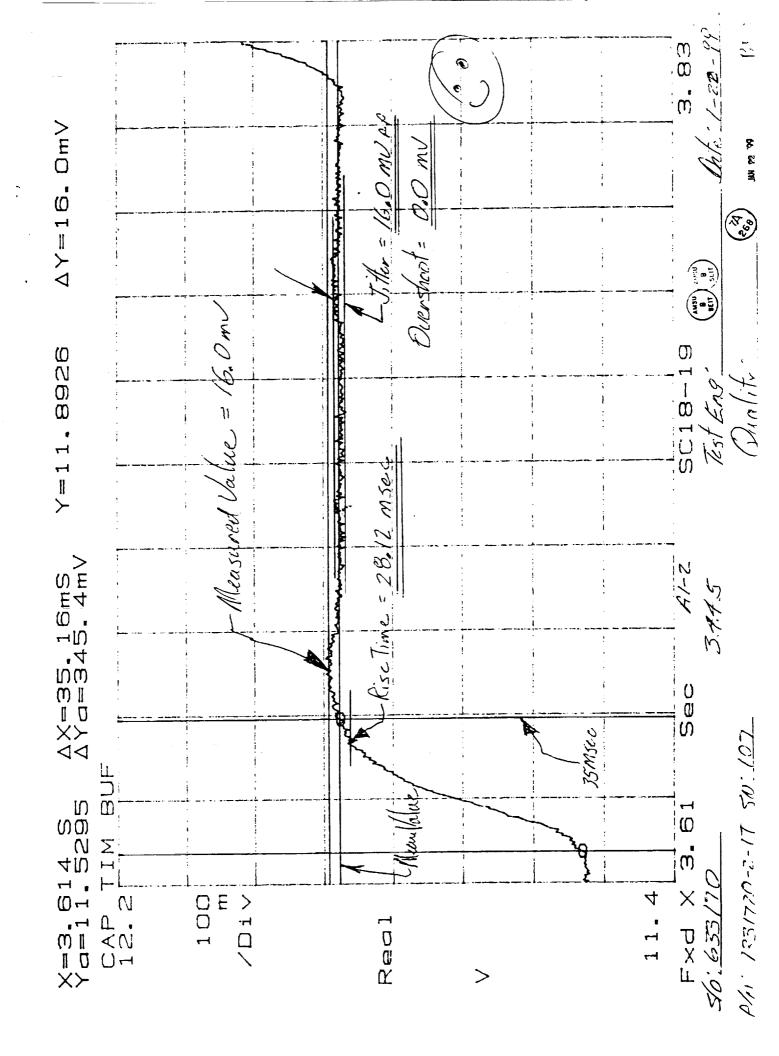


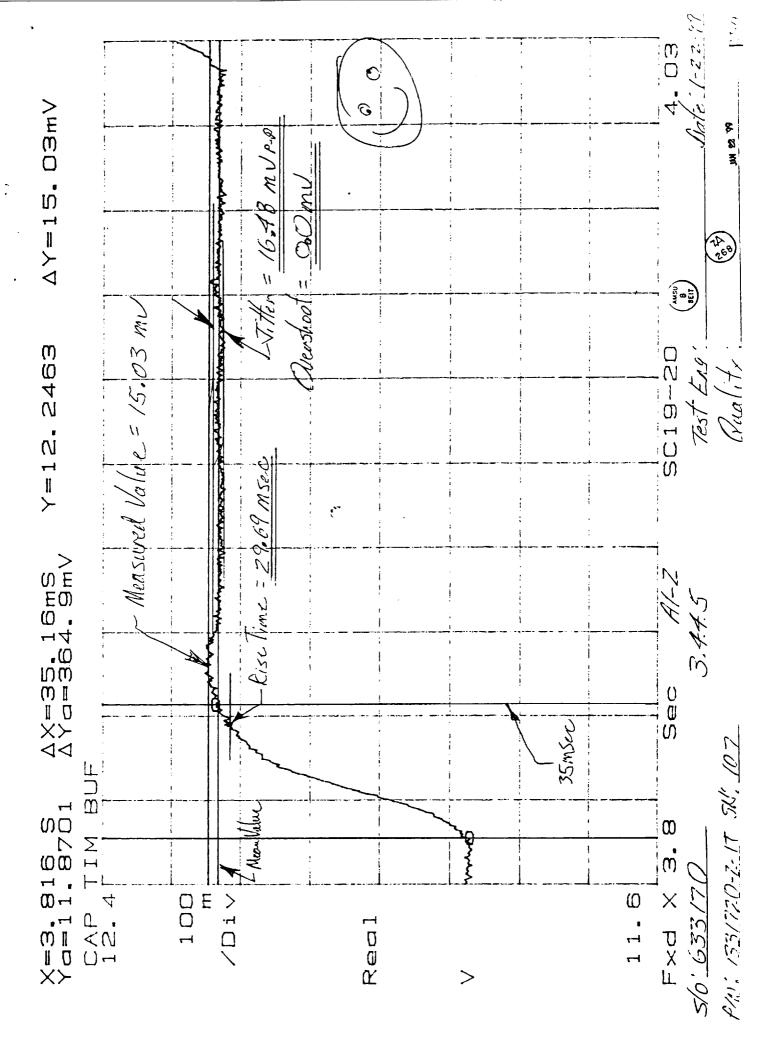


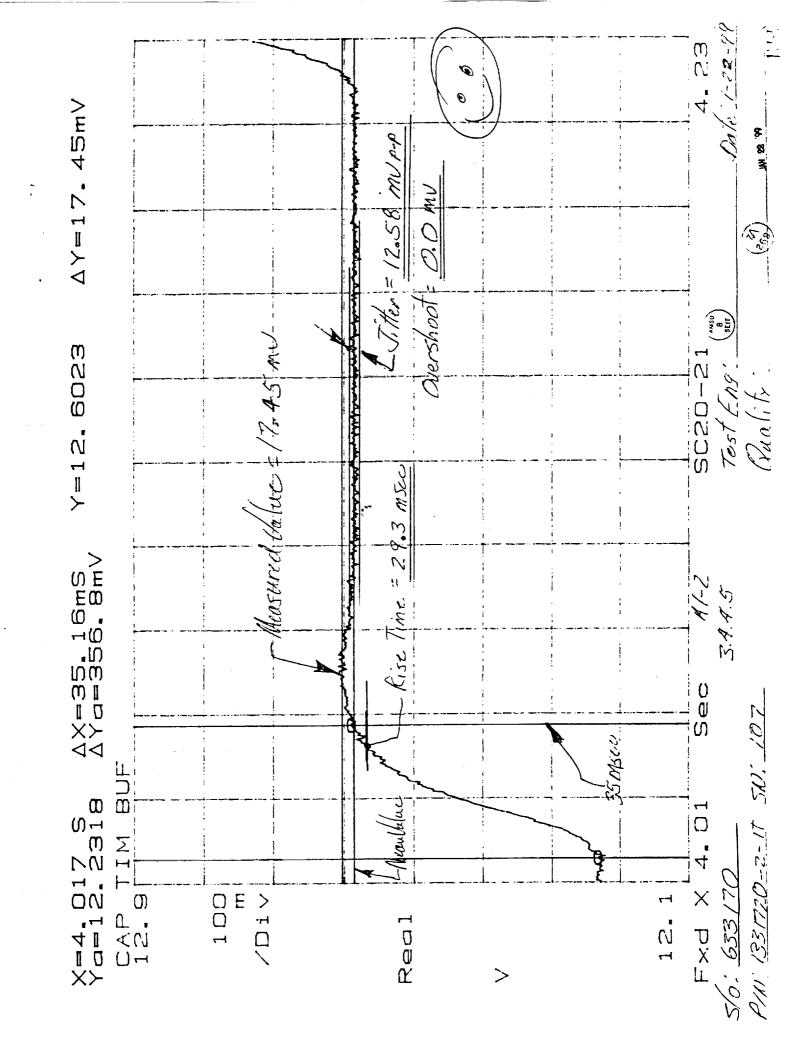


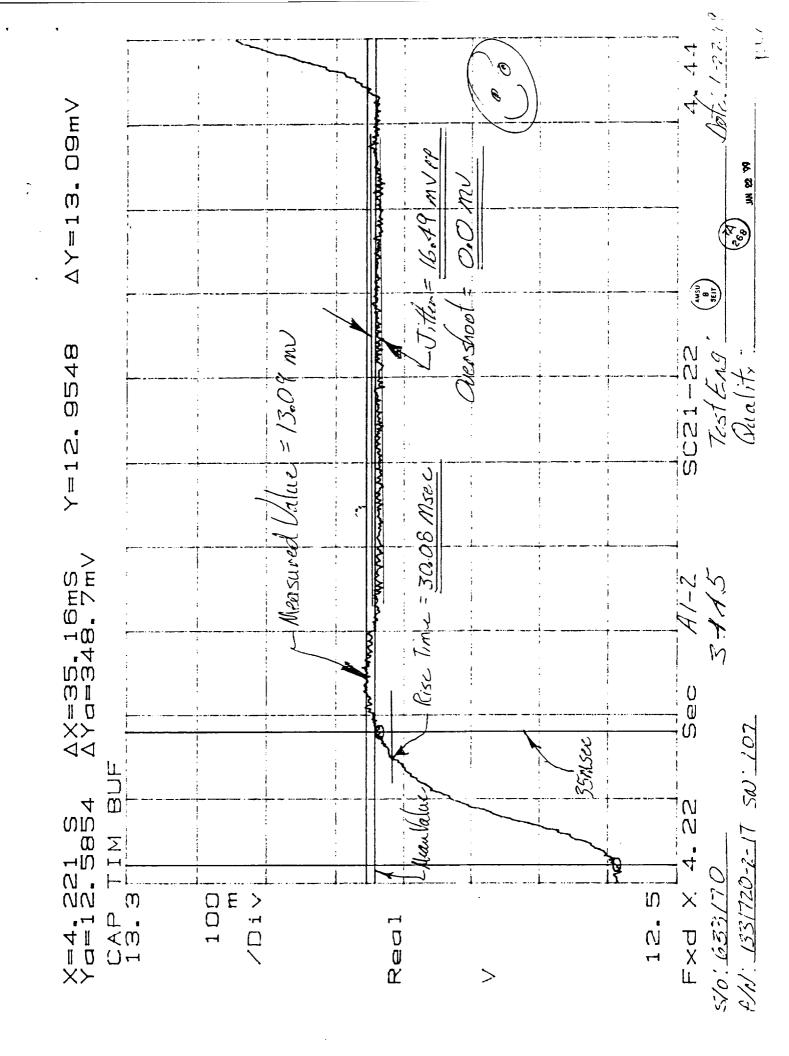


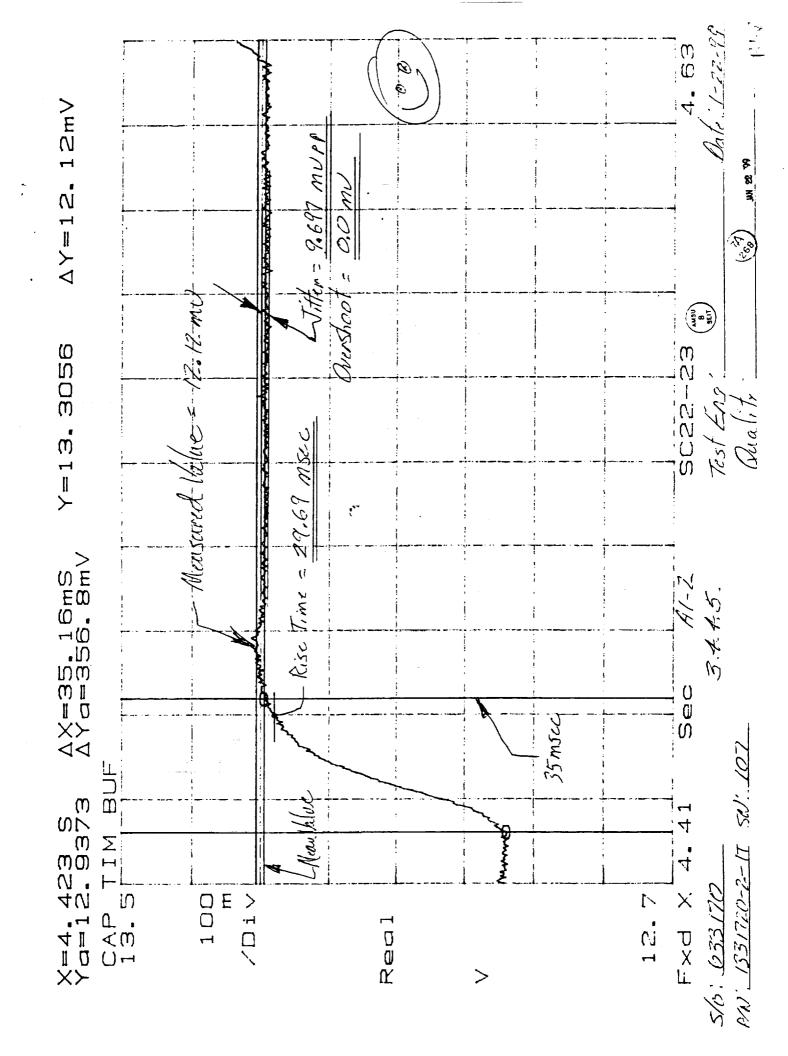


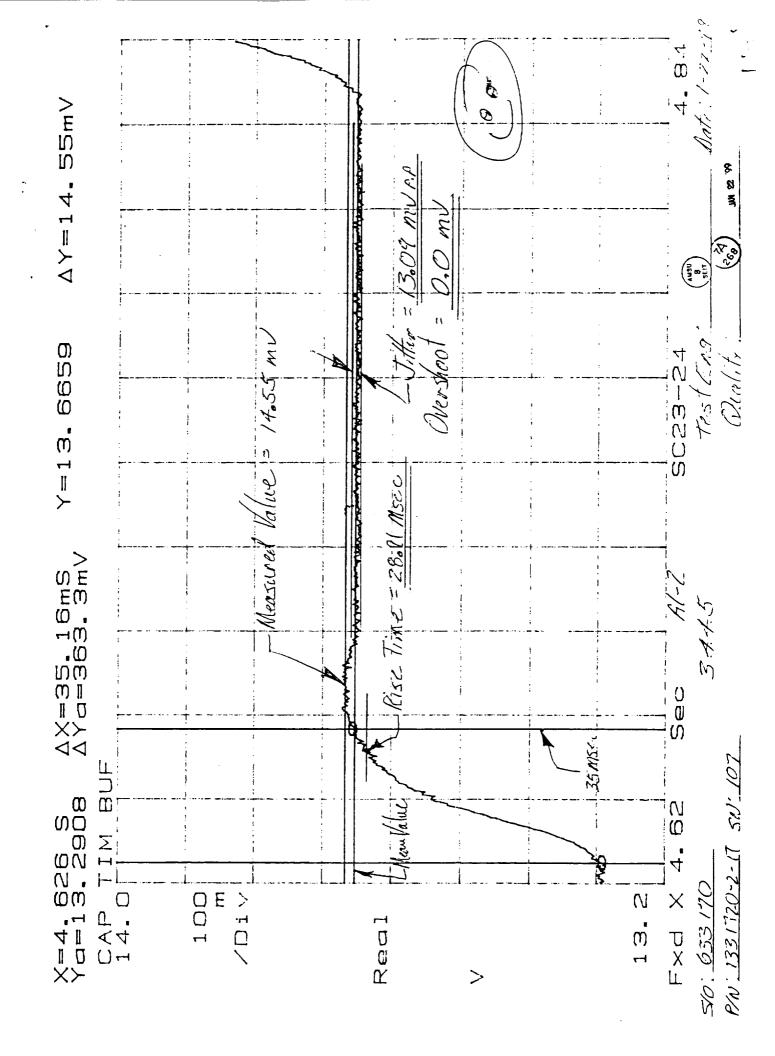


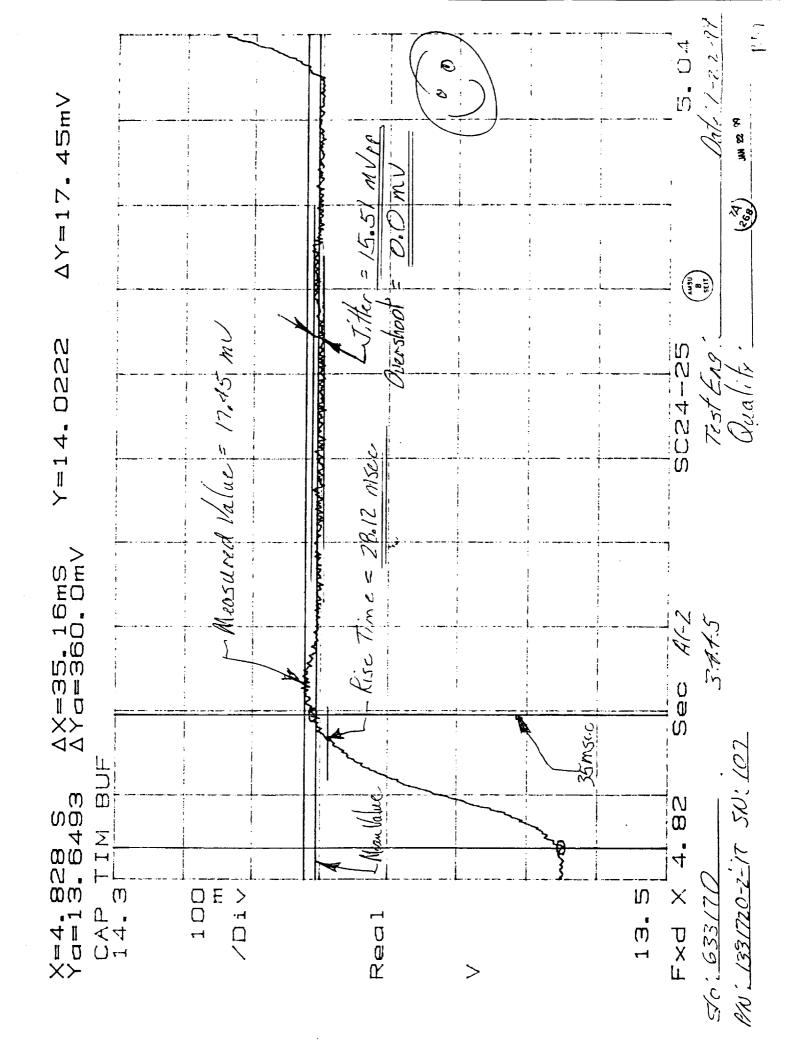


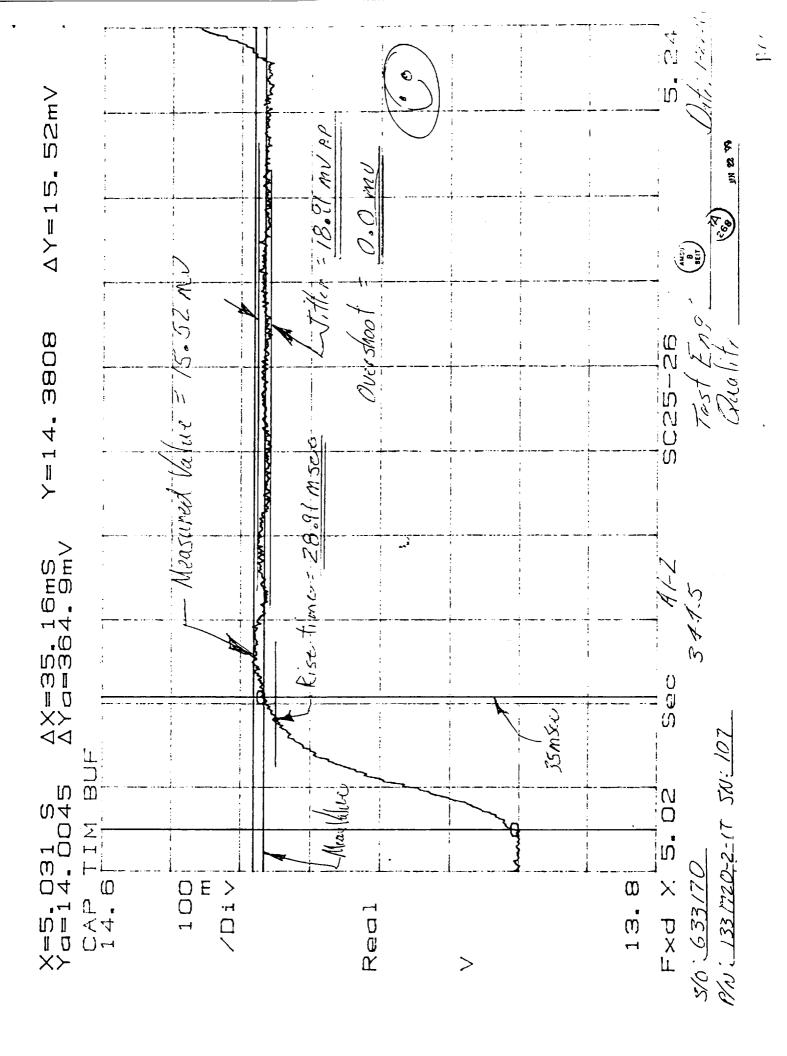


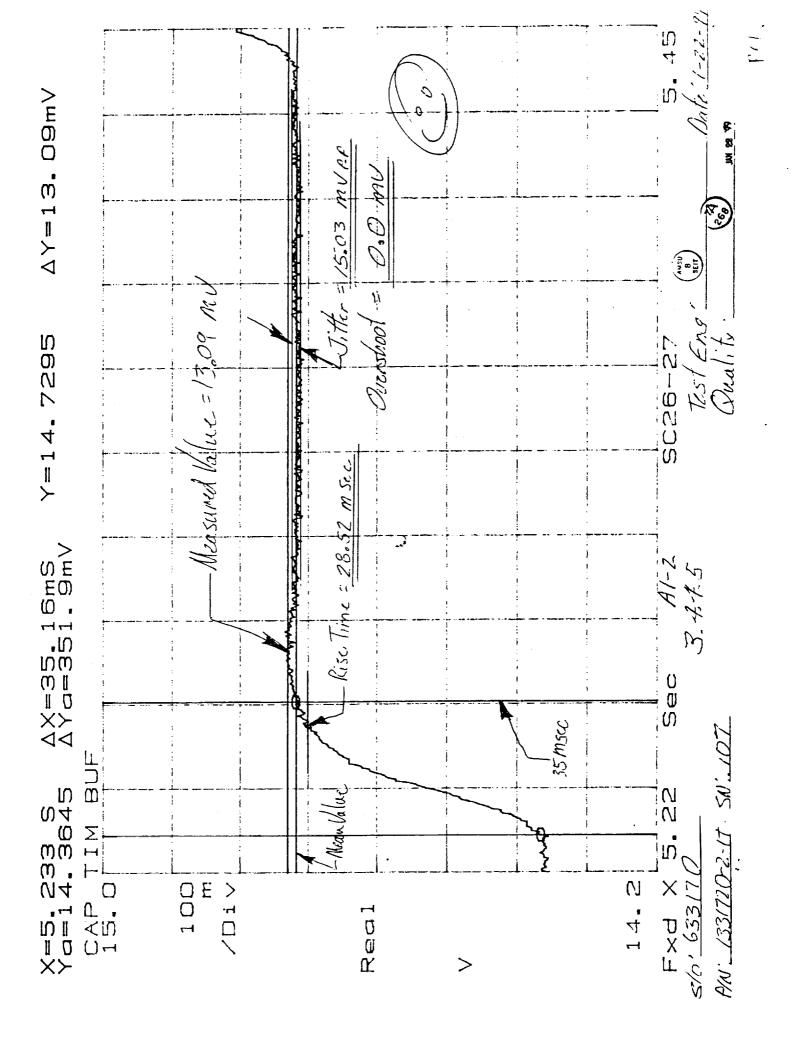


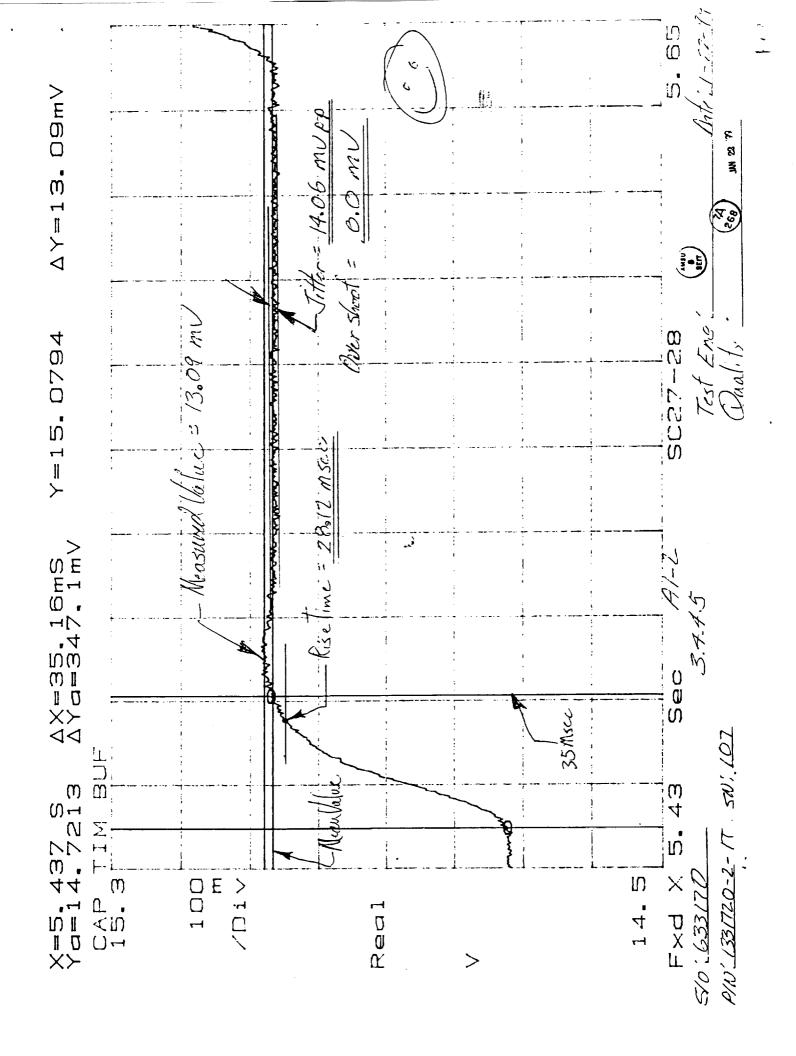


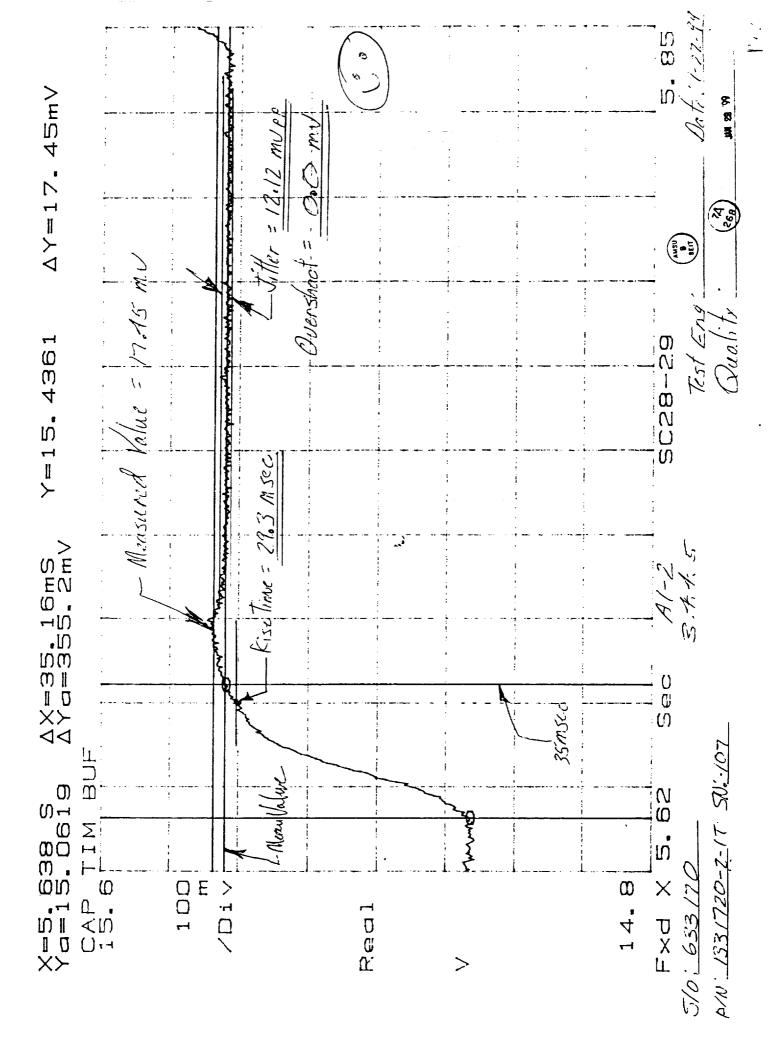


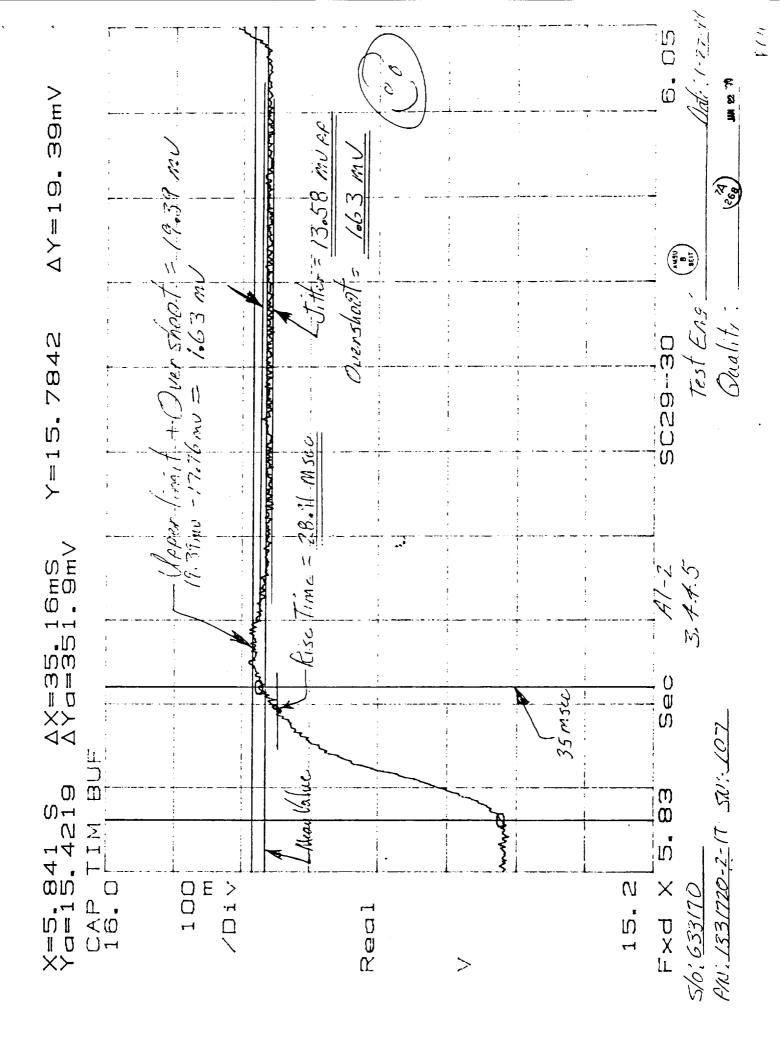


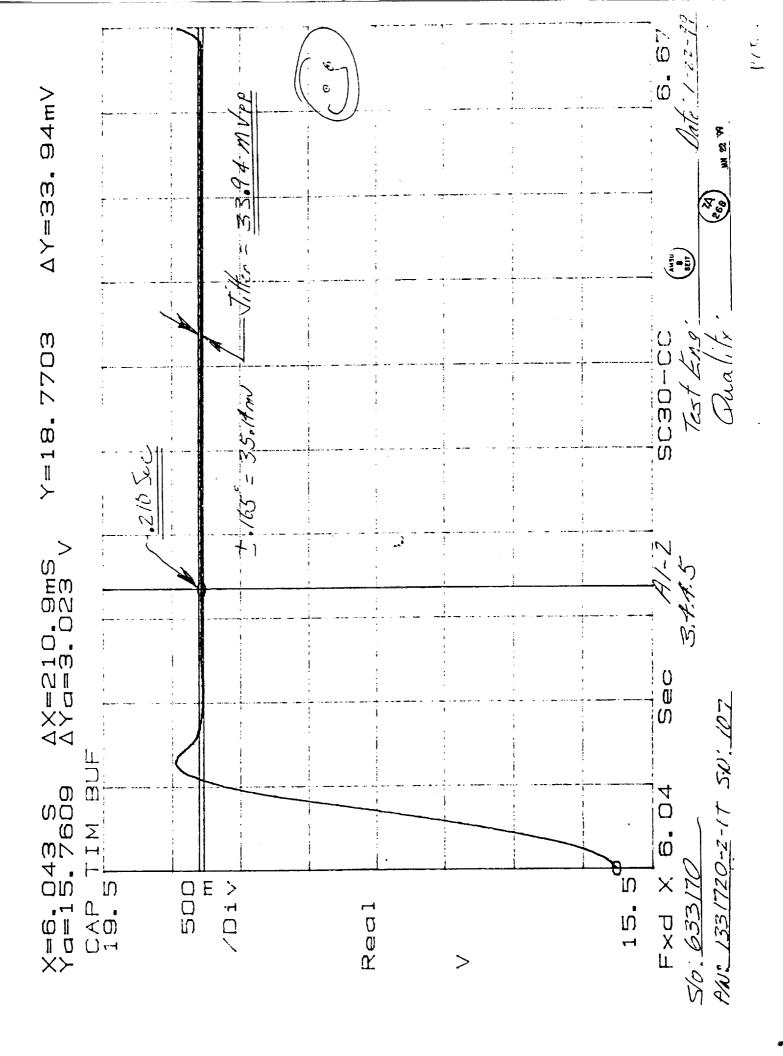


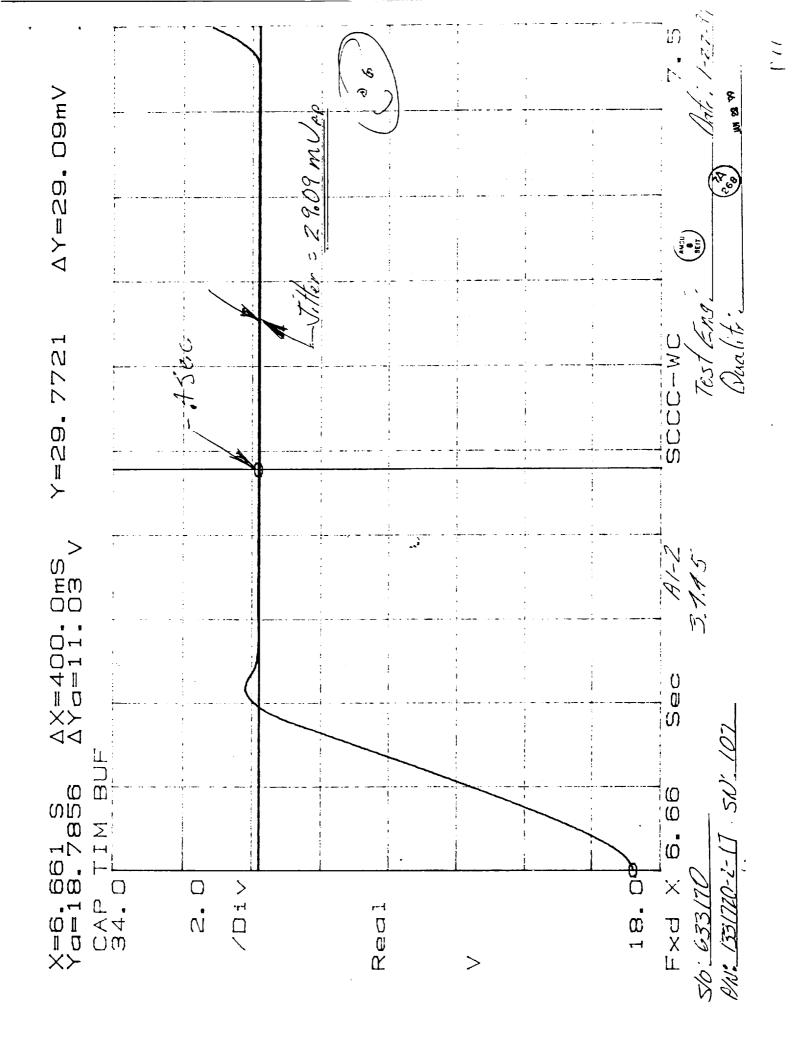












TEST DATA SHEET 7 (Sheet 1 Of 4) Scan Motion and Jitter Test (A1-1) (Paragraph 3.4.4.5)

Test Setup Verified: Kay AMALIA Shop Order No. 633/70
Signature

Step No.	Description	Requirement	Test Result	Pass/Fail
7		Stepping Slewing <8 sec period per Figure 8	< 8.0 Sec	P
9	Scene 1-2 3.33° step	<35 msec rise time per Figure 7	25.78 MSec	ıρ
		< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	11.25 mV 0.55 mV	P
10	Scene 2-3 3.33° step	<35 msec rise time per Figure 7	28.91 Mscc	P
		< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	8.533 mV	ρ
11	Scene 3-4 3.33° step	<35 msec rise time per Figure 7	26.95 Msec	P
	·	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	13.58 mu 3.65 mu	F
12	Scene 4-5 3.33° step	<35 msec rise time per Figure 7	30.47 Ms.c	P
	·	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	17.07 mV	f
13	Scene 5-6 3.33° step	<35 msec rise time per Figure 7	30-86 Mscc	P
	·	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	12.41 mV	P
14	Scene 6-7 3.33° step	<35 msec rise time per Figure 7	26.17 Msec	P
	·	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	8.146 mv	P
15	Scene 7-8 3.33° step	<35 msec rise time per Figure 7	27.73 Mscc	ρ
	·	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	13.19 MV	P
16	Scene 8-9 3.33° step	<35 msec rise time per Figure 7	27.73 Msec	ρ
	·	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	15.13 mu 3.65 mu	P

FIGURE TEST DATA SHEET 7 (Sheet 2 Of 4) Scan Motion and Jitter Test (A1-1)

Step No.	Description	Requirement	Test Result	Pass/Fai
17	Scene 9-10 3.33° step	<35 msec rise time per Figure 7	27.73 Mgcc	P
		< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	16,68 miv	F
18	Scene 10-11 3.33° step	<35 msec rise time per Figure 7	25-78 Msec	P
	•	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	14.74 mv 0.0 mv	F
19	Scene 11-12 3.33° step	<35 msec rise time per Figure 7	28.12 Msec	P
	·	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	12.41 mv 0.16 mv	P
20	Scene 12-13 3.33° step	<35 msec rise time per Figure 7	28.12 Msec	P
	·	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	17.64 MV	ρ
21	Scene 13-14 3.33° step	<35 msec rise time per Figure 7	27.73 Msec	P
	·	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	15.9 mv 0.0 mil	7
22	Scene 14-15 3.33° step	<35 msec rise time per Figure 7	28.52 Msec	P
		< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	14.74 mu 0.0 mv	P
23	Scene 15-16 3.33° step	<35 msec rise time per Figure 7	23.05 Mscc	P
	•	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	16.0 mV	P
24	Scene 16-17 3.33° step	<35 msec rise time per Figure 7	27.34 Mscc	F
	·	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	16.97 MV 123 MV	P

TEST DATA SHEET 7 (Sheet 3 Of 4) Scan Motion and Jitter Test (A1-1)

Step No.	Description	Requirement	Test Result	Pass/Fail
25	Scene 17-18 3.33° step	<35 msec rise time per Figure 7	28.52 Msec	P
	,	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	15.03 mu	P
26	Scene 18-19 3.33° step	<35 msec rise time per Figure 7	28.52 Misec	P
	0.00 0.00	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	17.45 mV	P
27	Scene 19-20 3.33° step	<35 msec rise time per Figure 7	26.56 Mscc	ß
		< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	16.97 mu	P
28	Scene 20-21 3.33° step	<35 msec rise time per Figure 7	28.52 Msec	P
	0.00 0.00	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	16.97 MV 4.23 MV	P
29	Scene 21-22 3.33° step	<35 msec rise time per Figure 7	26.17/1scc	P
	0.00 0.0	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	12.61 inv	P
30	Scene 22-23 3.33° step	<35 msec rise time per Figure 7	29.69 Mscc	P
	0.00 0.00	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	17.45 MV 0.0 MV	P
31	Scene 23-24 3.33° step	<35 msec rise time per Figure 7	27.34 Mscc	P
	0.00 0.00	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	18.42 mV	ρ
32	Scene 24-25 3.33° step	<35 msec rise time per Figure 7	26.56 mscc	P
	0.00 Stop	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	14.55 mu 4,23 mv	P

TEST DATA SHEET 7 (Sheet 4 Of 4) Scan Motion and Jitter Test (A1-1)

Step No.	Description	Requirement	Test Result	Pass/Fai
33	Scene 25-26 3.33° step	<35 msec rise time per Figure 7	26.56 Misco	β
		< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	18-12 MU 1.81 MU	P
34	Scene 26-27 3.33° step	<35 msec rise time per Figure 7	27.73 Msec	P
	·	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	19.39 MU	P
35	Scene 27-28 3.33° step	<35 msec rise time per Figure 7	26.95 Mscc	P
		< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	16.0 MW 2.78 MW	P
3 6	Scene 28-29 3.33° step	<35 msec rise time per Figure 7	28.12 Misec	P
		< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	15.52 MV	P
37	Scene 29-30 3.33° step	<35 msec rise time per Figure 7	27-73 Mscc	P
	·	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	16.0 MV 1.32 MV	P
38	Scene 30 Cold Cal	<0.21 sec slew time per Figure 10	<.21 Sec	P
	35.0° slew	< ±0.165° jitter per Figure 11	33.7mv	P
39	Cold Cal - Warm Cal	<0.40 sec slew time per Figure 12	<.40scc	P
	96.67° slew	< ±0.165° jitter per Figure 13	29.09 mv	ρ

Unit:/33/720-2-17	Test Engineer:
Serial No.: / 0 7	Quality Assurance: (7A) 1-33-99
Date: 1-22-99	Customer Representative: DR 218 99

TEST DATA SHEET 8 (Sheet 1 Of 4) Scan Motion and Jitter Test (A1-2) (Paragraph 3.4.4.5)

Test Setup Verified: Cut Arthur Shop Order No. 633/70

Step No.	Description	Requirement	Test Result	Pass/Fai
44		Stepping Slewing <8 sec period per Figure 8	< 8.0 Sec	P
9	Scene 1-2 3.33° step	<35 msec rise time per Figure 7	29.3 Mec	<i>p</i>
		< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	10.47 mV 0.0 mu	P
10	Scene 2-3 3.33° step	<35 msec rise time per Figure 7	29.69 Mer	ρ
	·	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	15.9 mu 1.25 mu	P
11	Scene 3-4 3.33° step	<35 msec rise time per Figure 7	30.86 Mscc	P
	•	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	15.13 mV 0.0 mv	P
12	Scene 4-5 3.33° step	<35 msec rise time per Figure 7	30.86 Mxc	P
	·	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	15.9 MV	P
13	Scene 5-6 3.33° step	<35 msec rise time per Figure 7	28,91 Mscc	P
	·	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	12.02 mu 0.0 mv	P
14	Scene 6-7 3.33° step	<35 msec rise time per Figure 7	29.69 Msec	P
	•	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	14.74 mV	P
15	Scene 7-8 3.33° step	<35 msec rise time per Figure 7	27,73 Msec	P
	•	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	15.51 mu 0.47 mu	f
16	Scene 8-9 3.33° step	<35 msec rise time per Figure 7	28.57 Mscc	A
	2,22	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	19.01 MV 3,96 MV	P

TEST DATA SHEET 8 (Sheet 2 Of 4) Scan Motion and Jitter Test (AI-2)

Step No.	Description	Requirement	Test Result	Pass/Fail
17	Scene 9-10 3.33° step	<35 msec rise time per Figure 7	28.91 macc-	P
		< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	15.52 MV	P
18	Scene 10-11 3.33° step	<35 msec rise time per Figure 7	29.3 Msec	P
		< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	18.23 MV 5.9 MV	ß
19	Scene 11-12 3.33° step	<35 msec rise time per Figure 7	26.91 Mese	P
		< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	15.19 MU 3.19 MV	1
20	Scene 12-13 3.33° step	<35 msec rise time per Figure 7	30.97 Msec.	P
	·	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	17.45 MV	P
21	Scene 13-14 3.33° step	<35 msec rise time per Figure 7	29.69 Macc	P
		< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	19-68 MU 0-0 mV	P
22	Scene 14-15 3.33° step	<35 msec rise time per Figure 7	30.86 Msec	P
		< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	16.97 mu 2.12 my	P
23	Scene 15-16 3.33° step	<35 msec rise time per Figure 7	28.52 Asec	P
		< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	11015 mu 5.03 MV	P
24	Scene 16-17 3.33° step	<35 msec rise time per Figure 7	28.71 Msec	B
		< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	13.57 mg 3.09 MU	P

TEST DATA SHEET 8 (Sheet 3 Of 4) Scan Motion and Jitter Test (A1-2)

Step No.	Description	Requirement	Test Result	Pass/Fail
25	Scene 17-18 3.33° step	<35 msec rise time per Figure 7	28.12 MECC	P
	, 0.00 0.0p	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	15.52 mu 0.18 mu	P
26	Scene 18-19 3.33° step	<35 msec rise time per Figure 7	28.12 Msiec	P
	•	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	16.0 MJ	P
27	Scene 19-20 3.33° step	<35 msec rise time per Figure 7	29.69 Msec	P
•	•	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	16.48 MU 0.0 MU	ρ
28	Scene 20-21 3.33° step	<35 msec rise time per Figure 7	29.3 Misec	f _
		< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	12.58 mu 0.0 mu	ρ
29	Scene 21-22 3.33° step	<35 msec rise time per Figure 7	30.08 Msec	P
	,	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	16.79 MV 0.0 mu	P
30	Scene 22-23 3.33° step	<35 msec rise time per Figure 7	29.69 Msec	ρ
	•	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	9.697 mu	<i>P</i>
31	Scene 23-24 3.33° step	<35 msec rise time per Figure 7	28.91 Msec	P
	2322	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	13.09 MU 10.0 MU	P
32	Scene 24-25 3.33° step	<35 msec rise time per Figure 7	28.12 Msec	P
	•	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	15.51 ml	P

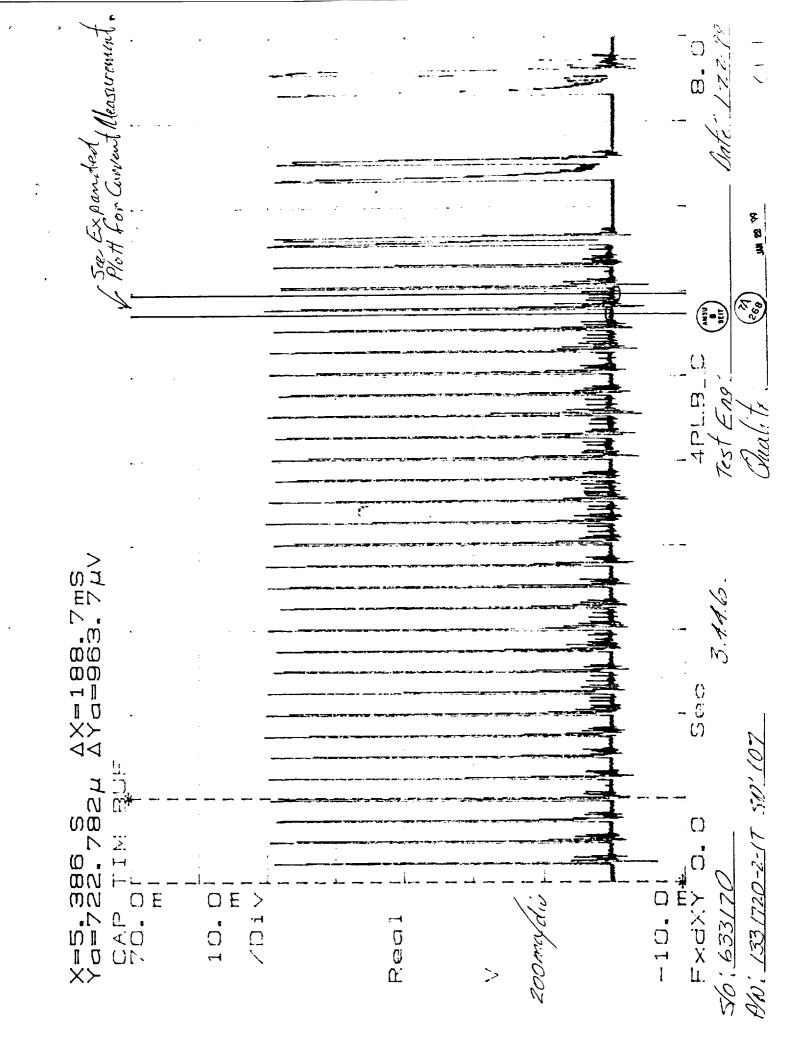
TEST DATA SHEET 8 (Sheet 4 Of 4) Scan Motion and Jitter Test (A1-2)

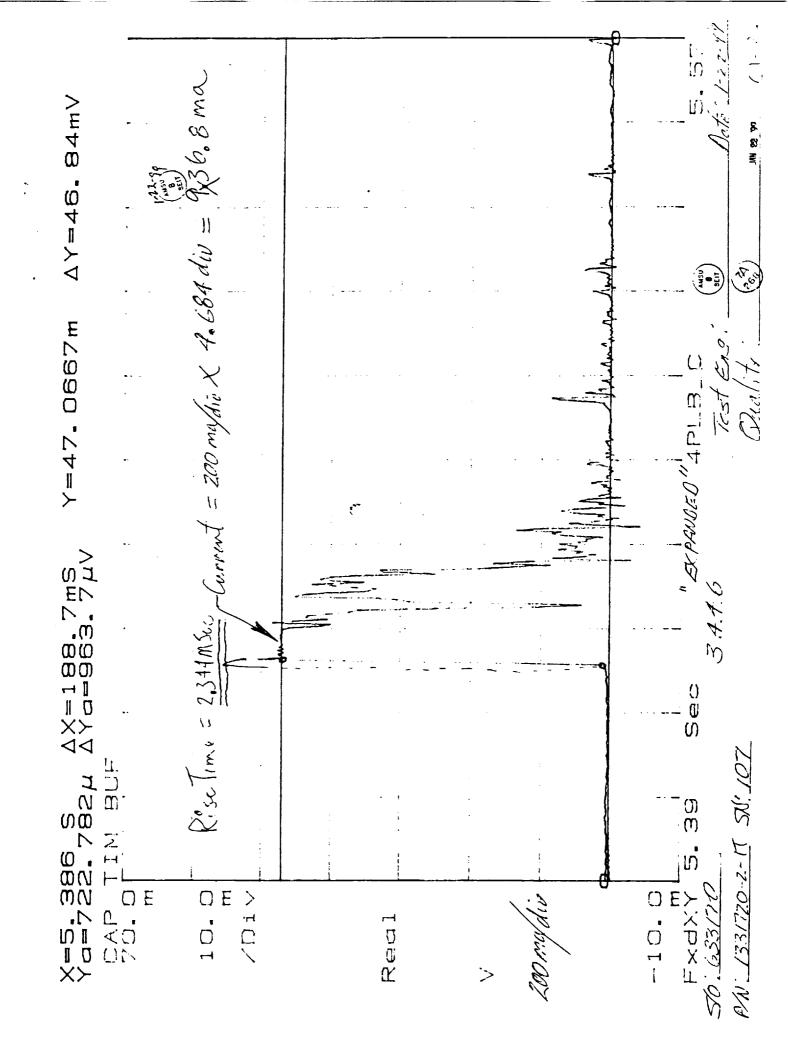
Step No.	Description	Requirement	Test Result	Pass/Fa
33	Scene 25-26 3.33° step	<35 msec rise time per Figure 7	28.91 m Sec	P
	·	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	18.91 mu 0.0 mu	P
34	Scene 26-27 3.33° step	<35 msec rise time per Figure 7	28.52 Msec	ρ
	·	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	15.03 MV	P
35	Scene 27-28 3.33° step	<35 msec rise time per Figure 7	28.12 Msec	P
	,	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	14.00 mu	P
36	Scene 28-29 3.33° step	<35 msec rise time per Figure 7	29.3 Msec	P
	·	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	12.12 mu 0.0 mu	P
37	Scene 29-30 3.33° step	<35 msec rise time per Figure 7	28.91 msec	P
	•	< ±5% jitter per Figure 7 < 3% overshoot for 10 msec	13.58 MV	P
38	Scene 30 Cold Cal	<0.21 sec slew time per Figure 10	20.21 Sec	P
	35.0° slew	< ±0.165° jitter per Figure 11	33.91 mu	P
39	Cold Cal - , Warm Cal	<0.40 sec slew time per Figure 12	< 0.4 Sec	ρ
	96.67° slew	< ±0.165° jitter per Figure 13	29.09 mu	F

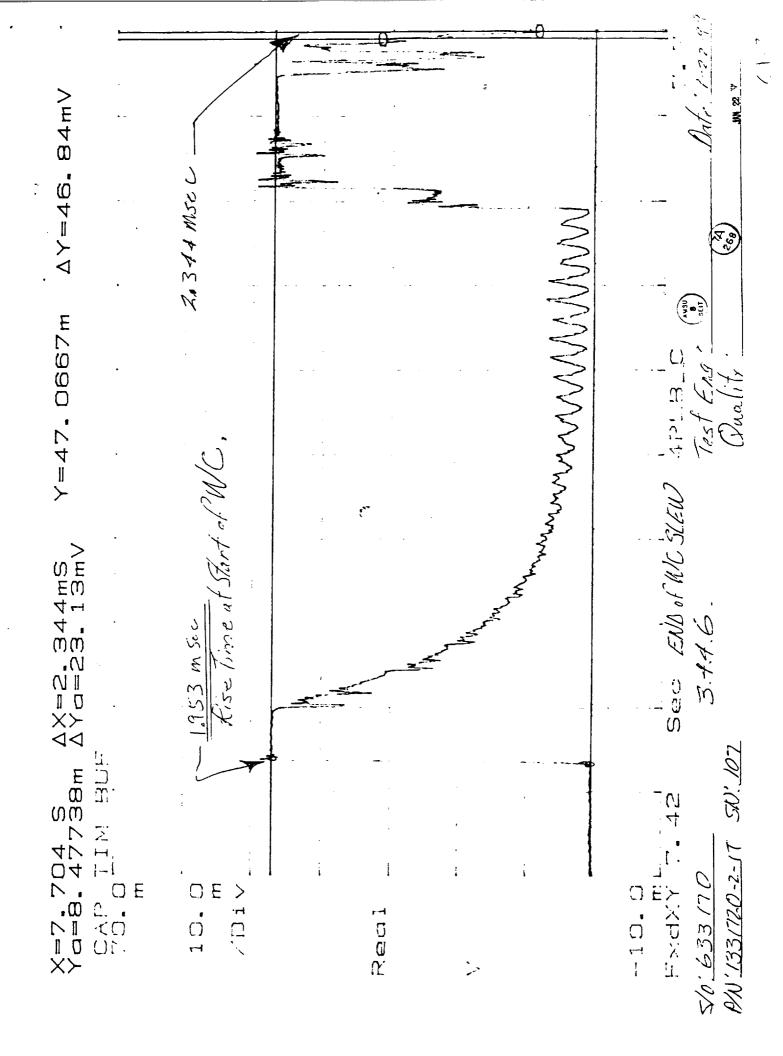
Unit: /33/720-2-/T	Test Engineer:
Serial No.: 107	Quality Assurance:
Date: 1-22-99	Customer Representative: 2 2 2/18/99

APPENDIX C

PULSE LOAD CURRENT WAVEFORM AND TEST DATA SHEET







28V Bus Peak Current and Rise Time Test (Paragraph 3.4.4.6)

	$\bigcap_{i=1}^{n}$.1/	Ω	
Test Setup Verified:	an I		219	7
	7 (1	Sign	ature	

Shop Order No. <u>633/70</u>

Step No.	Requirement	Test Result	Pass/Fail
4	< 1 A peak any place in the scan	936.8 ma	P
5	> 35 µsec rise time, 3.33° step	2.344 MSC	P
6	> 35 µsec rise time, start of WC slew	1.953 m Sec	P
6	> 35 µsec rise time, end of WC slew	2.344 MSec	P

•••

Pass = P Fail = F

Unit: <i>/33/720-2-1T</i>	
Serial No.:	

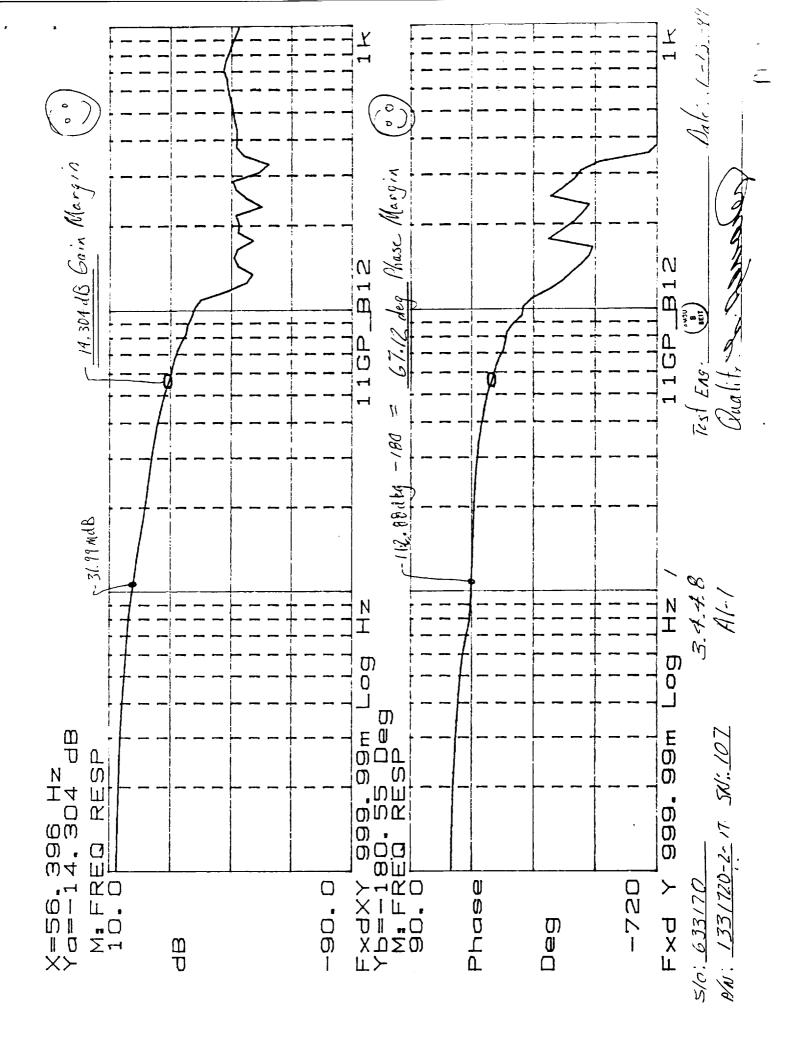
Test Engineer:	_
Quality Assurance: (593)	
Quality Assurance.	_

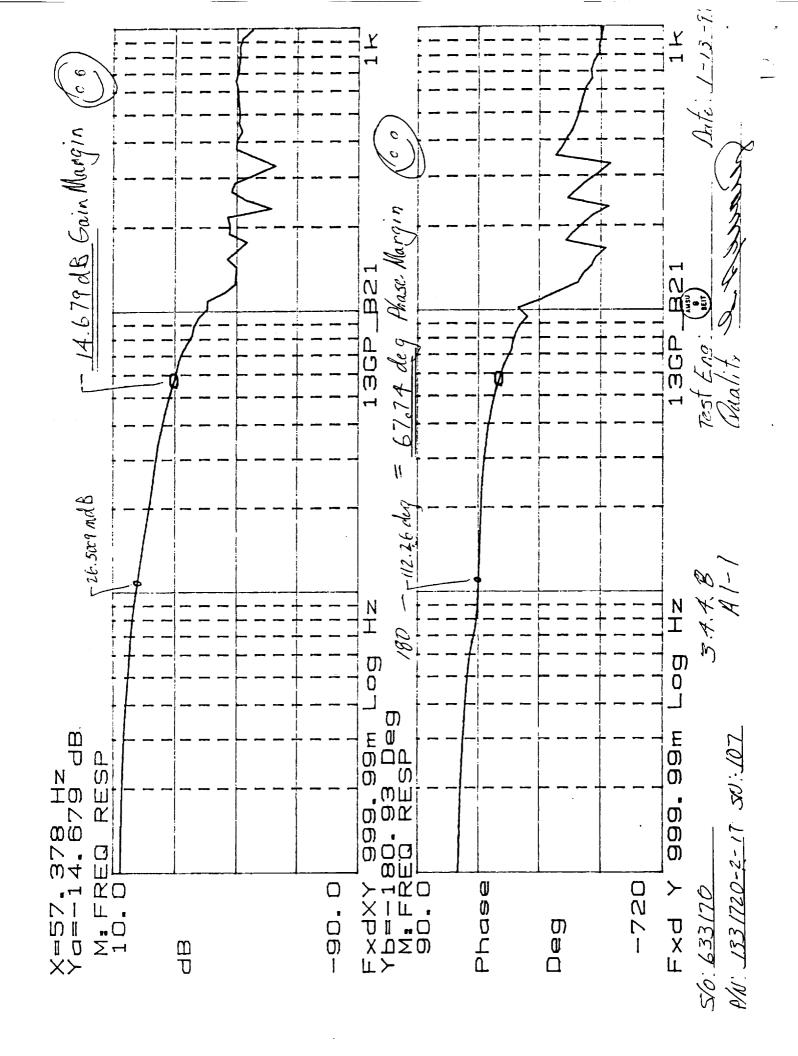
AMSU

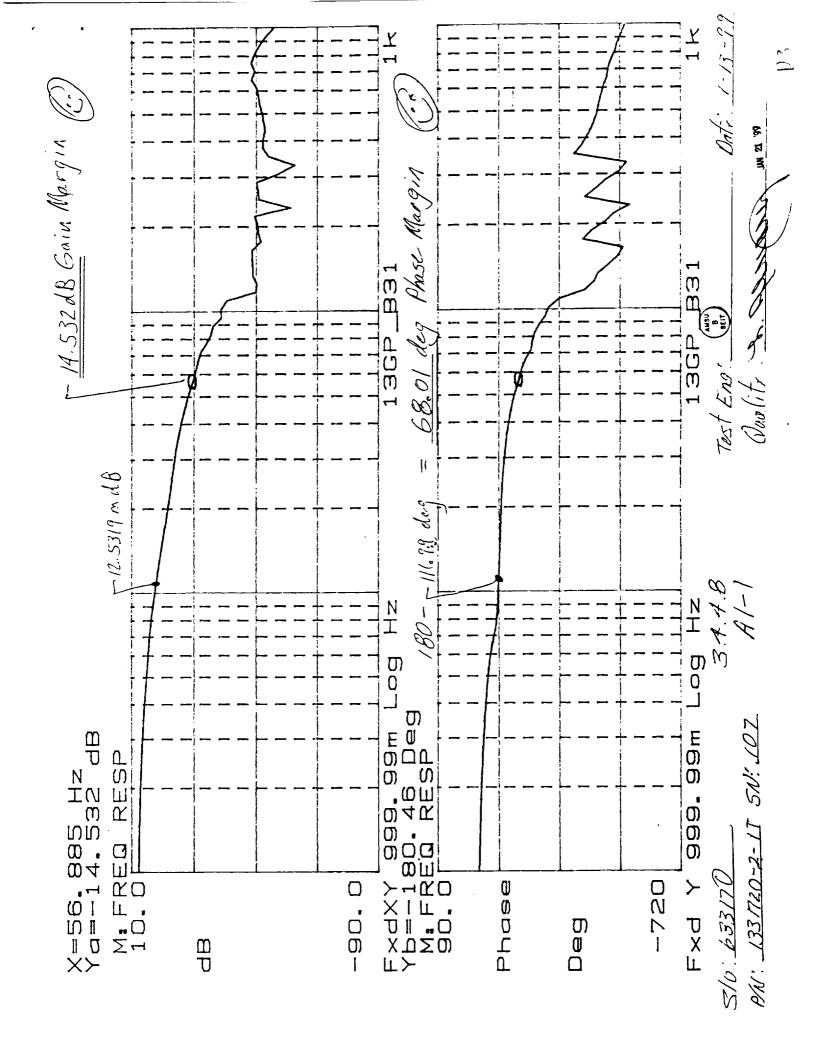
APPENDIX D

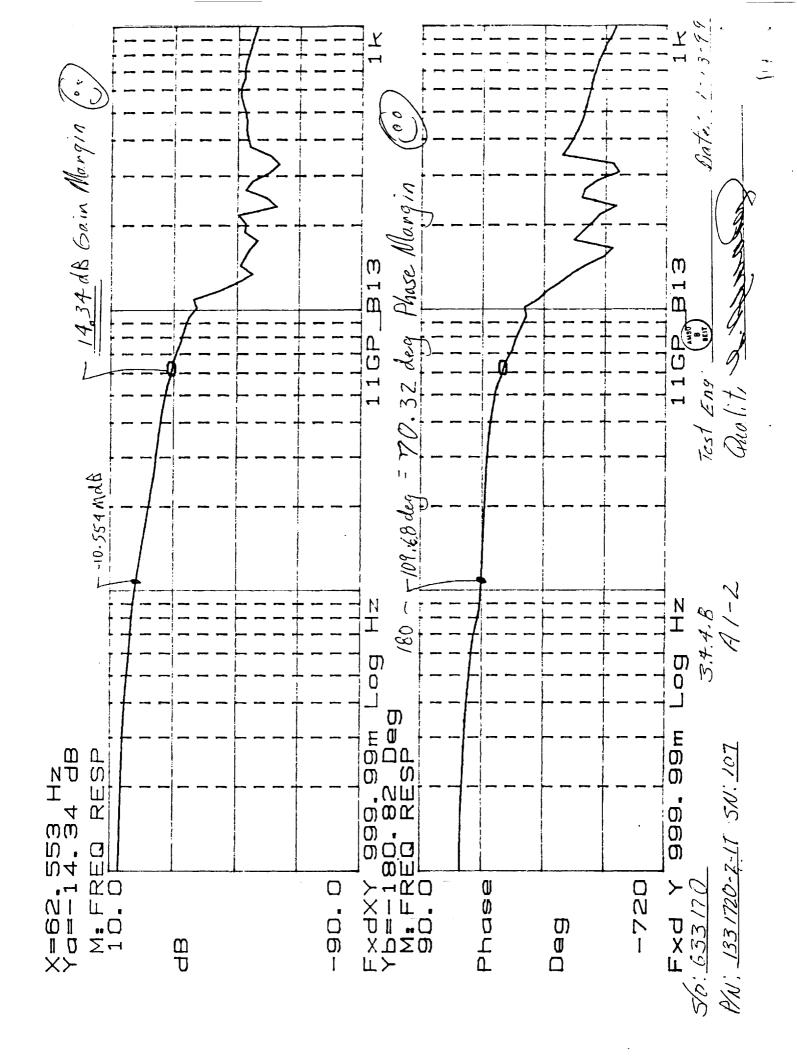
GAIN AND PHASE MARGIN PLOTS AND TEST DATA SHEETS

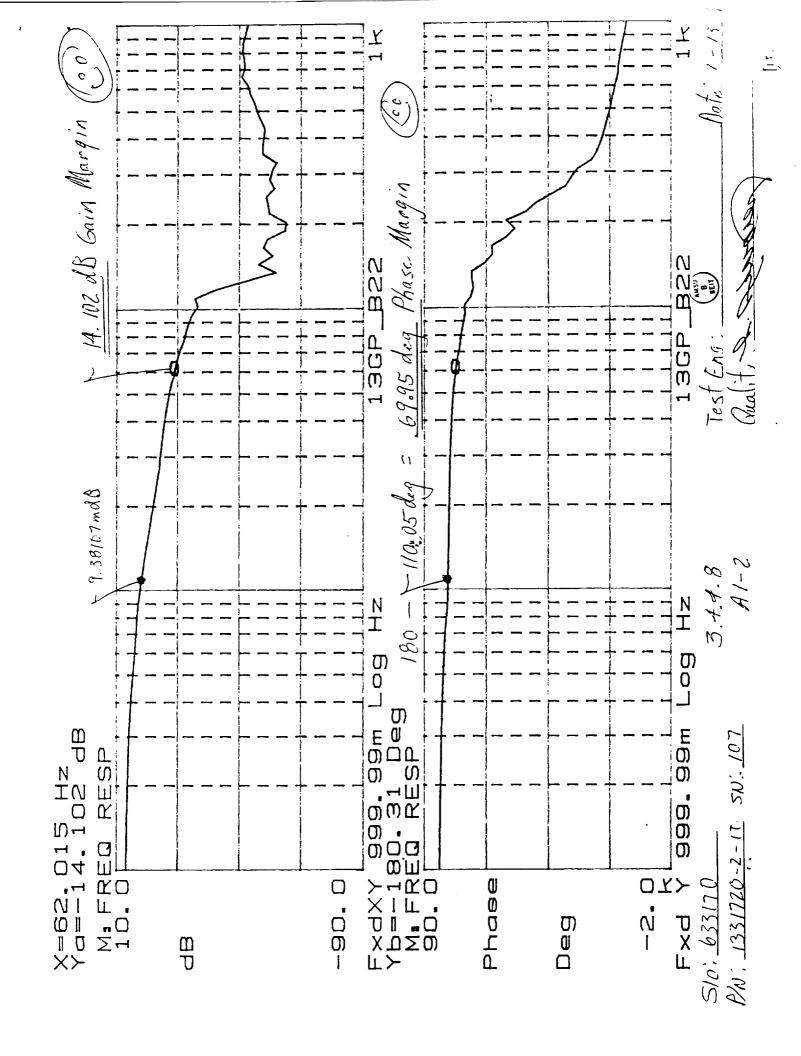
	S	Swept Sine		
AVERAGE.	INTGRT TIME	Д	# AVGS	
FREQ. START STOP	999, 99 mHz 1 kHz	N	SPAN RESLTN	3.0 Dec 33.3 Pt/Dc
SWEEP.	TYPE Log	DIR.	EST TIME 9.17 Min	EST RATE 183 S/Dc
AU GAIN	0 f f			
IN N N N N N N N N N N N N N N N N N N	RANGE AutoRng↑ AutoRng↑	ENG UNITS 1.0 V/EU 1.0 V/EU	COUPLING DC (F1t) DC (F1t)	
SOURCE:	TYPE Off		LEVEL 1.0 Vpk	0FFSET 0.0 <pre>0.0</pre>
5/0: 633/70 P/N: 133/720-2-17: 50: 107		3.4.48 A1-1 and A1-2	Test Ens ()	Jak: 1-13-21

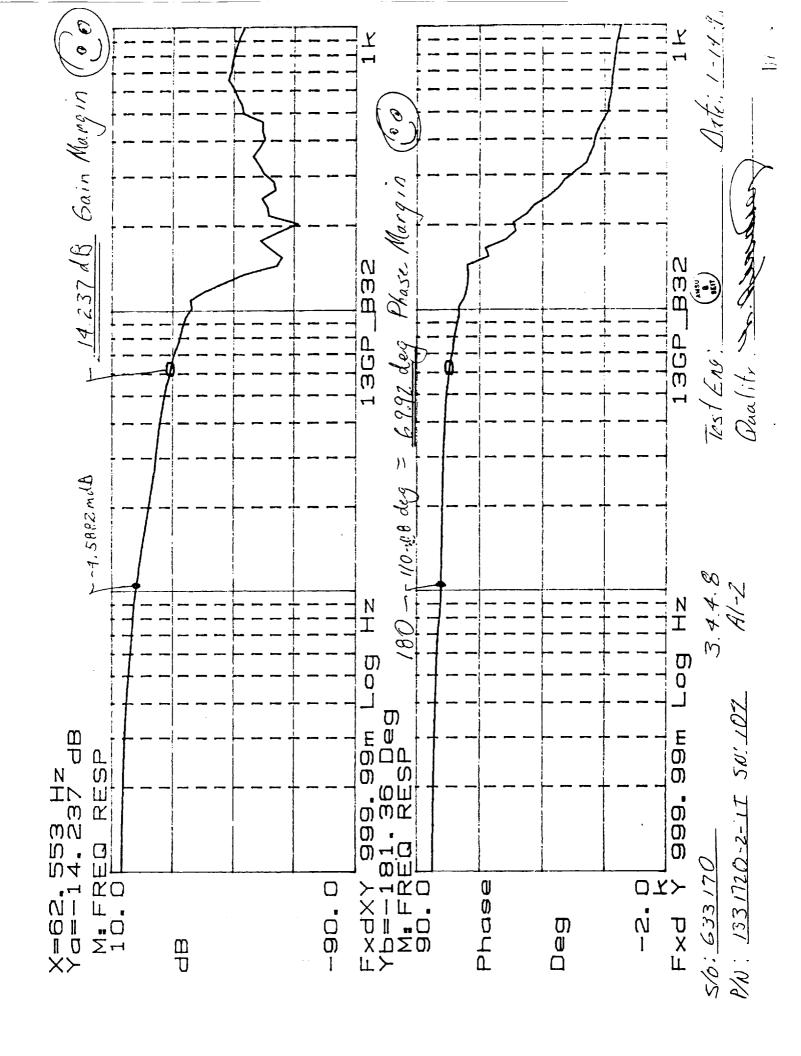












Gain/Phase Margin (A1-1) (Paragraph 3.4.4.8)						
Test Setup Verified: Markhusa Shop Order No. 633/70 Signature Temperature: 68.5 °C						
Temperature:	<u>00.0</u> °C					
	Requirement	Test Result	Pass/Fail			
	9.2 dB minimum	1 14.304 dB 2 14.679 dB 3 14.532 dB	P			
	25 degrees minimum	1 67.12 deg 2 67.74 deg 3 68.01 des	ß			
				Pass = P Fail = F		
Serial No.:	3/720-2-17 107 -22-99	~	JAN 28 79	Alays (m		

Test Setup Veri	0 ##	Shop Order No. <u>633/70</u>	 -	
Temperature:	<u>68.5°</u> €			
	Requirement	Test Result	Pass/Fail	
	9.2 dB minimum	1 14.34 dB 2 14.102 dB 3 14.237 dB	ρ	
	25 degrees minimum	1 70.32 deg 2 69.95 deg 3 69.92 des	P	
				Pass = P Fail = F
Unit:/33 / Serial No.:/6 Date:/ - 2		Test Engineer: Quality Assurance: Customer Representative:) s	m 28 79 ~> 2 8 99
	.			

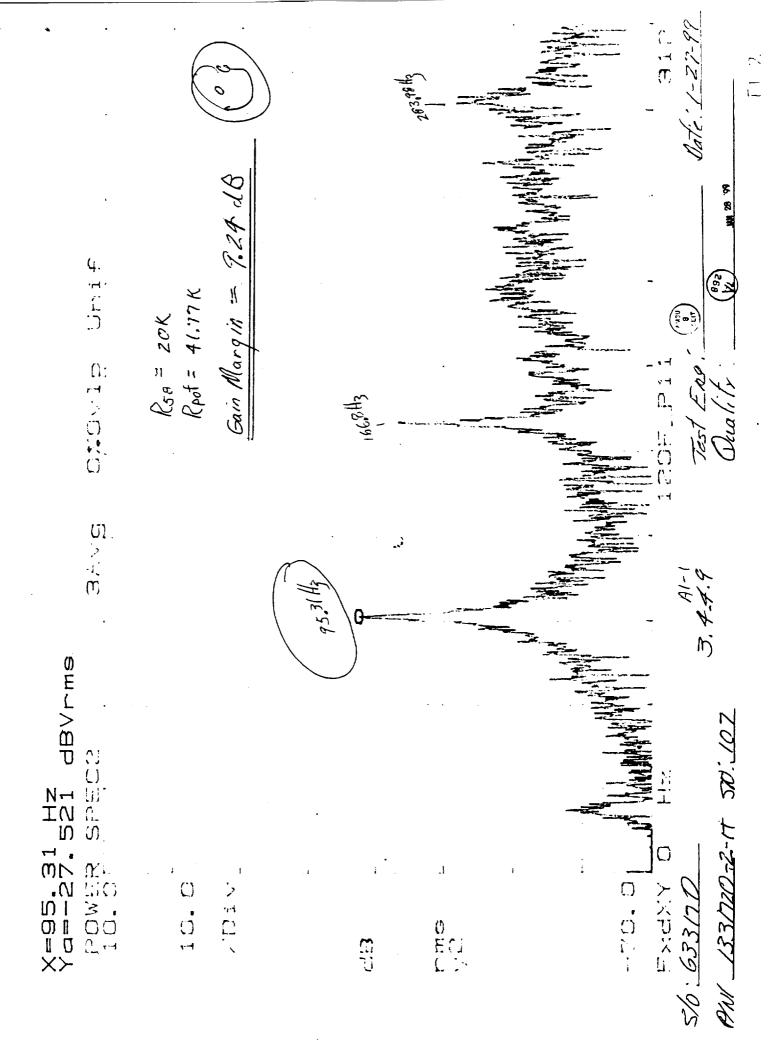
APPENDIX E

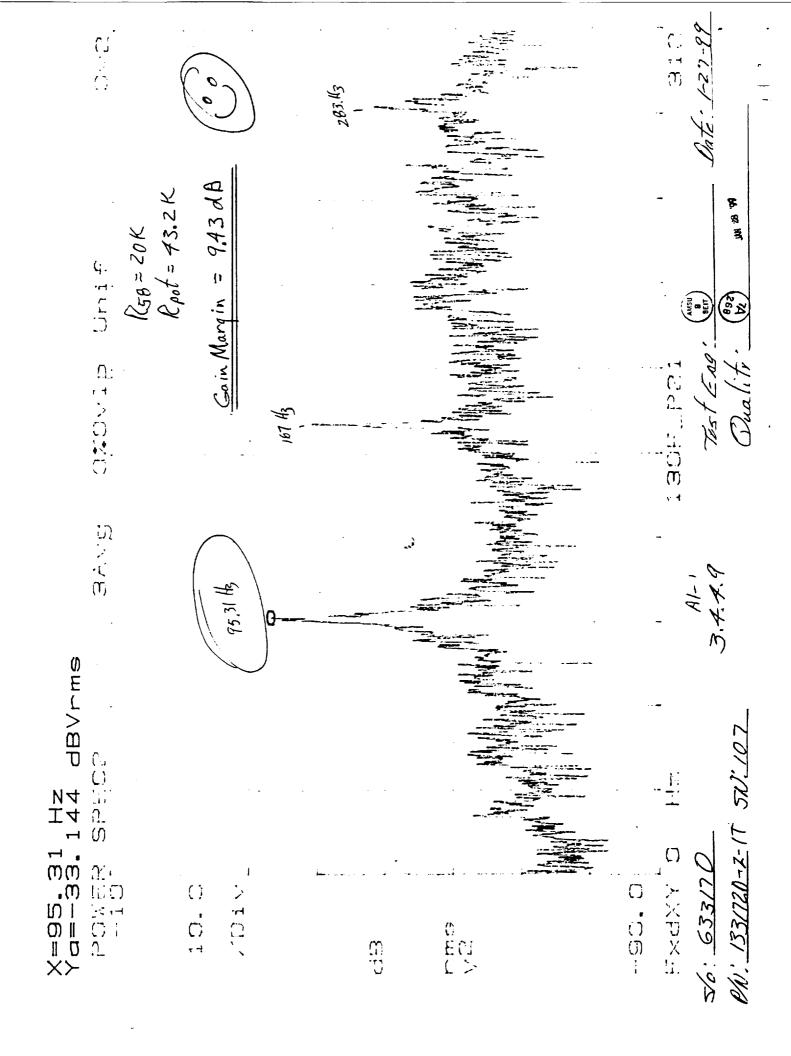
OPERATIONAL GAIN MARGIN POWER SPECTRUM PLOTS AND TEST DATA SHEETS

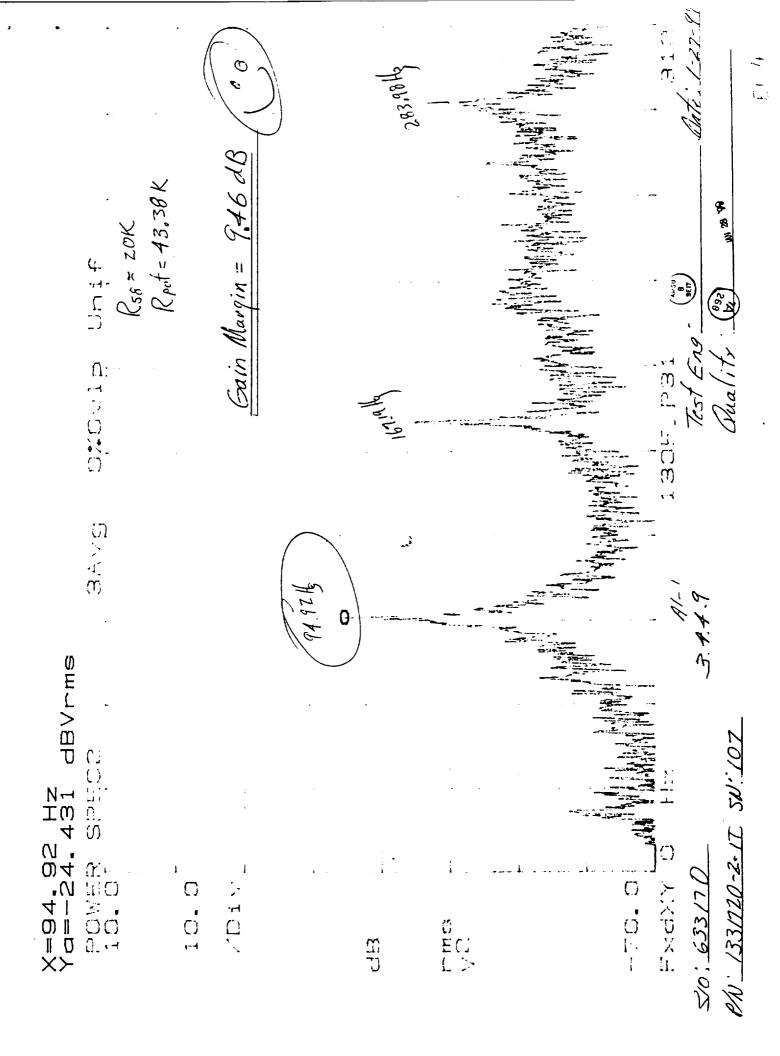
Linear Resolution

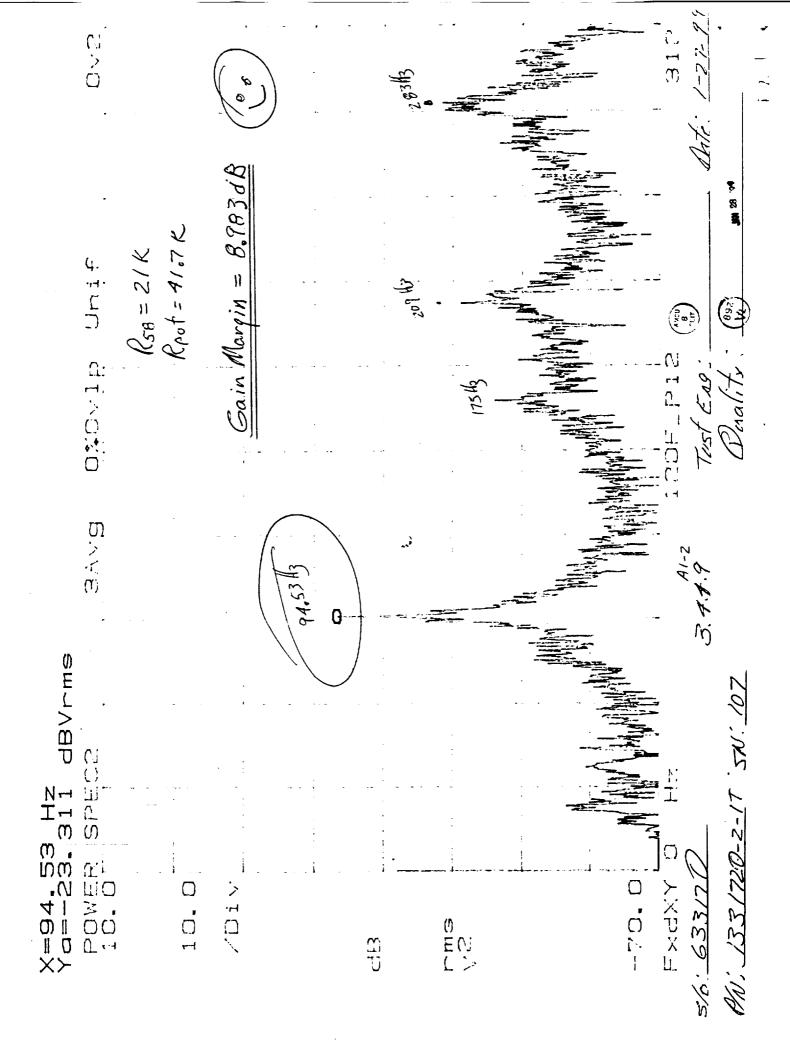
!

MEASURE	CHAN 1 OFF		CHAN 2 Power Spec	0
WINDOW.	CHAK 1 Uniform		CHAN 2 Uniform	
AVERAGE	TYPE Stable	# AVGS	OVERLAP OX	TIME AVG Off
rred.	CENTER 150.00 HE		SPAN 312 Hz	BW 3GimHE
•	REC LGTH 2.56 S	At t 1.25mS		
TRIGGER.	TYPE Chan 2	LEVEL O.O VPK	SLOPE	PRESTEW OFF
INPUT CH CH CH CH CH CH CH CH CH CH CH CH CH	RANGE Autorna Autorna	ENG UNITS 1.0 V/EU 1.0 V/EU	COUPLING DC (FIt) DC (FIt)	DELAY 0.0 S 0.0 S
SOURCE:	五十二年五日十二十二十二十二十二十二十二十二十二十二十二十二十二十二十二十二十二十二十二		LEVEL O.O VOR	OFFISHT O.O VOR
56: 633/70 PAV: 133/720-2-17 SAV: 107	3.44.9 N: 1027	A1-1	Test Ens; (1)	Date: 1-26-99

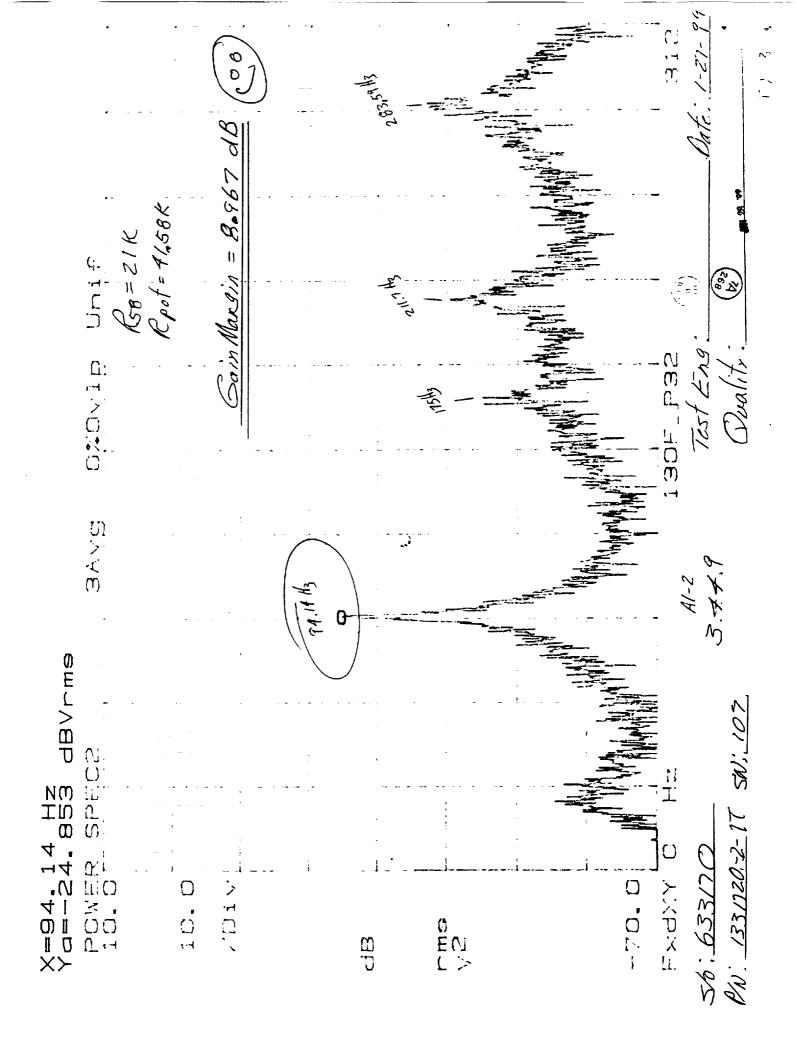








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TXDX7 D TIX



Operational Gain Margin (A1-1) (Paragraph 3.4.4.9)

Test Setup Verified: Jay Hulley	Shop Order No. <u>633/70</u>
Signature	-
Temperature: 6/08°C	

Step No.	Requirement		Test Result	Pass/Fail
	R58 Resistance (kohms)		20 K	
11		1	41.77 K	
	Test Pot Resistance (kohms)	2	43.2 K	
	,	3	43.38 K	
		1	95.31 H3	
12	Oscillation Frequency (Hz)	2	95.31 K	
		3	94.97 H3	
		1	9.24 dB	
16	Gain Margin, 8 dB minimum	2	9.43 dB	$\Box \rho$
.0		3	7.46 1R	•

	(Arriv
Unit: /33/720-2-17	Test Engineer:
Serial No.: 107	Quality Assurance: (268) 28 %
	Date: 1-27-99

		Operational Gain M	(argin (A1-2) (Paragraph 3.4.4.9)	
	Setup Verific	' I Signature	op Order No. <u>633/70</u>	
Tem	perature: <u>6</u> 1	<u>1.8°</u> €		
	Step No.	Requirement	Test Result	Pass/Fail
	Olep No.	R58 Resistance (kohms)	21 K	1 45571 411
	11	Test Pot Resistance (kohms)	1 41.7 K 2 42.46 K 3 41.58 K	P
	12	Oscillation Frequency (Hz)	1 94.53 H ₃ 2 94.14 H ₃ 3 94.14 H ₃ 1 8.383 dB)	P
	16	Gain Margin, 8 dB minimum	1 8.783 dB) 2 9.08 dB 3 8.967 dB	- P
	,	720-2-17	Test Engineer: (AMSU B SELT) TAA 268	Pass = P Fail = F
Serial I	No.: <i>_/C</i>	<u>7</u>	Quality Assurance: 268 Date: 1-27-99	2 **

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